AL-AMEEN ENGINEERING COLLEGE

(AUTONOMOUS)

KARUNDEVANPALAYAM, ERODE – 638 104.

LABORATORY RECORD

Name : ____________________________ ____________

Register No. : ______________________________________

Class : ____________________ ________________

Code & Subject : ______________________________________

AL-AMEEN

ENGINEERING COLLEGE

(AUTONOMOUS)

KARUNDEVANPALAYAM, ERODE – 638 104.

Department of

LABORATORY RECORD

Name : ……………………………………………… Roll No. : …………………………

Reg. No: ……………………………………………… Year / Sem : ……………………….....

Certified that this is the Bonafide Record of work done by the above student in the………………….. Laboratory during the year ………………….

STAFF INCHARGE **HEAD OF THE DEPARTMENT**

Submitted for the University Practical Examination held on ________________

INTERNAL EXAMINER **EXTERNAL EXAMINER**

CONTENTS

S.No.	Date	Name of the Experiments	Page No.	Marks	Signature with Date

Internal Marks:

AL-AMEEN ENGINEERING COLLEGE

(AUTONOMOUS)

(Accredited by NAAC with "A" Grade :: An ISO Certified Institution)

Erode – 638 104.

MARKS AWARDED BASED ON RUBRICS

Course Code & Title:

____

Expt. / Ex. No.	Marks Awarded					
	Diagram & Formula (2)	Skill Level & Tabulation (3)	Calculation & Results (2)	Viva (2)	Attitude (1)	Total Marks (10)
Total Marks						

Marks (Out of 80)	

Faculty Signature

SYLLABUS

OBJECTIVES:

To learn design, testing and characterizing of circuit behavior with digital and analog ICs.

LIST OF EXPERIMENTS

1. Implementation of Boolean Functions, Adder and Subtractor circuits.
2. Code converters: Excess-3 to BCD and Binary to Gray code converter and vice-versa
3. Parity generator and parity checking
4. Encoders and Decoders
5. Counters: Design and implementation of 3-bit modulo counters as synchronous and Asynchronous types using FF IC's and specific counter IC.
6. Shift Registers: Design and implementation of 4-bit shift registers in SISO, SIPO, PISO, PIPO modes using suitability IC's.
7. Study of multiplexer and de multiplexer
8. Timer IC application: Study of NE/SE 555 timer in Astability, Monostability operation.
9. Application of Op-Amp: inverting and non-inverting amplifier, Integrator and Differentiator.
10. Voltage to frequency characteristics of NE/ SE 566 IC.

ADDITIONAL EXPERIMENTS:

1. Study of flip flops

LIST OF EXPERIMENTAL SETUP

I CYCLE:

1. Study of basic digital ICs.
2. Implementation of Boolean Functions
3. Adder/ Subtractor circuits.
4. Excess-3 to BCD and Binary to Gray code converter and vice-versa
5. Parity generator and parity checker
6. Encoders and Decoders
7. Multiplexer and demultiplexer
8. Design and implementation of 4-bit shift registers in SISO, SIPO, PISO, PIPO modes using suitable IC's.

II CYCLE:

9. Design and implementation of 4-bit asynchronous up counter using FF IC.
10. Design and implementation of BCD synchronous counter using FF IC.
11. Timer IC application: Study of NE/SE 555 timer in Astable, Monostable operation
12. Application of Op-Amp: inverting and non-inverting amplifier.
13. Application of Op-Amp:Adder,comparator, Integrator and Differentiator.
14. Voltage to frequency characteristics of NE/ SE 566 IC.
15. Study of flip flops

Ex.No: **STUDY OF BASIC DIGITAL ICs**

Date:

AIM: To verify the truth table of basic digital ICs of AND, OR, NOT, NAND, NOR, EX-OR gates.
APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	AND gate	IC 7408	1
3.	OR gate	IC 7432	1
4.	NOT gate	IC 7404	1
5.	NAND gate	IC 7400	1
6.	NOR gate	IC 7402	1
7.	EX-OR gate	IC 7486	1
8.	Connecting wires	As required	

THEORY:

a. AND gate:

An AND gate is the physical realization of logical multiplication operation. It is an electronic circuit which generates an output signal of ‘1’ only if all the input signals are ‘1’.

b. OR gate:

An OR gate is the physical realization of the logical addition operation. It is an electronic circuit which generates an output signal of ‘1’ if any of the input signal is ‘1’.

c. NOT gate:

A NOT gate is the physical realization of the complementation operation. It is an electronic circuit which generates an output signal which is the reverse of the input signal. A NOT gate is also known as an inverter because it inverts the input.

d. NAND gate:

A NAND gate is a complemented AND gate. The output of the NAND gate will be ‘0’ if all the input signals are ‘1’ and will be ‘1’ if any one of the input signal is ‘0’.

e. NOR gate:

A NOR gate is a complemented OR gate. The output of the OR gate will be ‘1’ if all the inputs are ‘0’ and will be ‘0’ if any one of the input signal is ‘1’.

f. EX-OR gate:

An Ex-OR gate performs the following Boolean function,

$$A \oplus B = (A B') + (A'B)$$

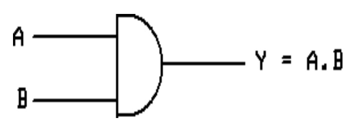
It is similar to OR gate but excludes the combination of both A and B being equal to one. The exclusive OR is a function that give an output signal ‘0’ when the two input signals are equal either ‘0’ or ‘1’.

PROCEDURE:

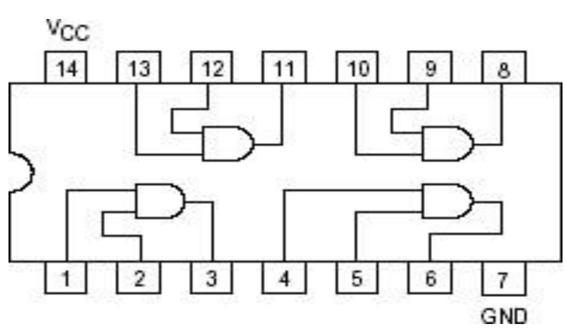
1. Connections are given as per the circuit diagram
1. For all the ICs 7th pin is grounded and 14th pin is given +5 V supply.
2. Apply the inputs and verify the truth table for all gates.

ANDGATE

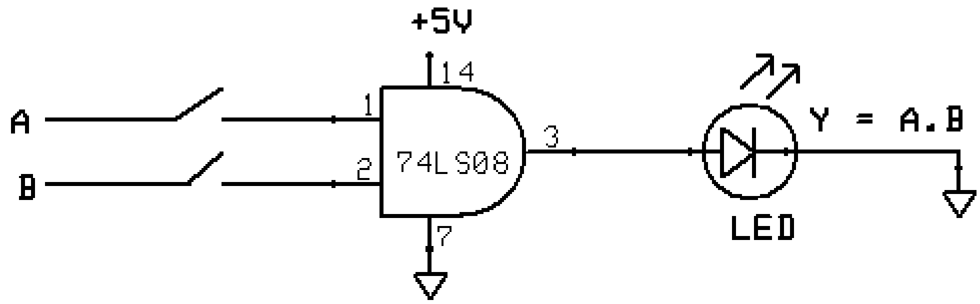
LOGIC DIAGRAM:



PIN DIAGRAM OF IC 7408:



CIRCUIT DIAGRAM:

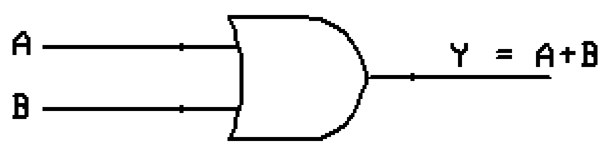


TRUTH TABLE:

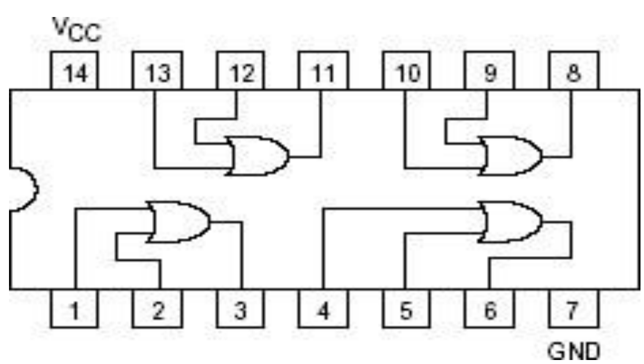
S.No	INPUT		OUTPUT
	A	B	Y = A. B
1.	0	0	0
2.	0	1	0
3.	1	0	0
4.	1	1	1

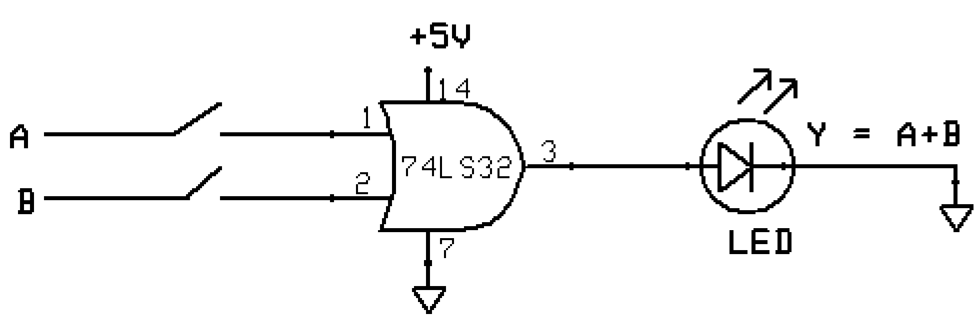
OR GATE

LOGIC DIAGRAM:



PIN DIAGRAM OF IC 7432 :



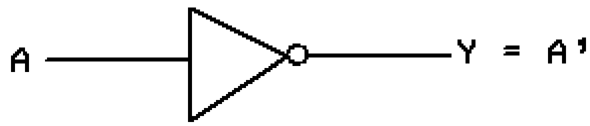


TRUTH TABLE:

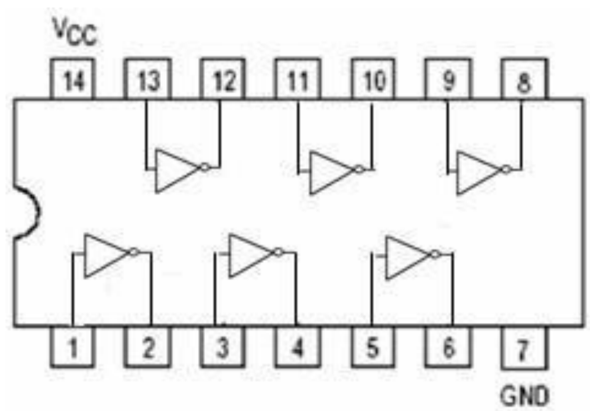
S.No	INPUT		OUTPUT
	A	B	Y = A + B
1.	0	0	0
2.	0	1	1
3.	1	0	1
4.	1	1	1

NOT GATE

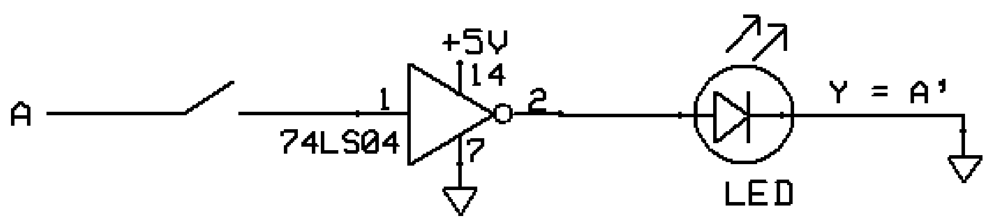
LOGIC DIAGRAM:



PIN DIAGRAM OF IC 7404 :



CIRCUIT DIAGRAM



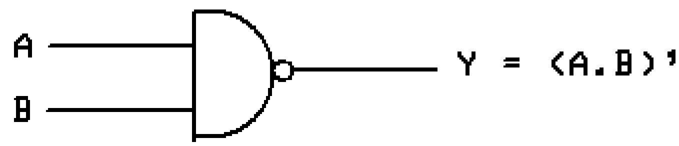
TRUTH TABLE:

S.No	INPUT	OUTPUT
	A	Y = A'
1.	0	1

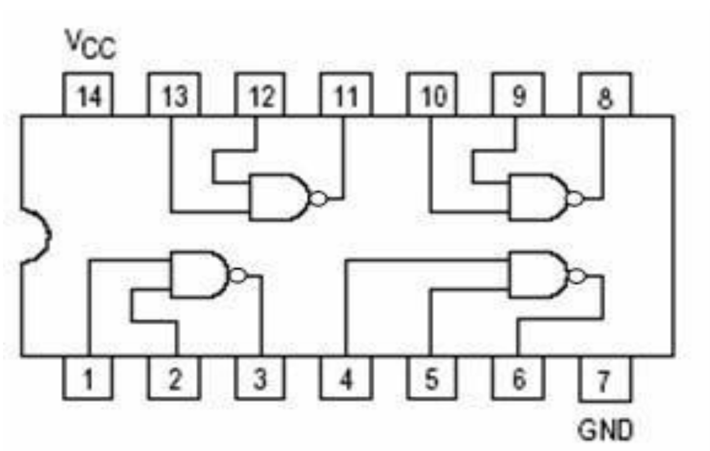
2.	1	0

NANDGATE

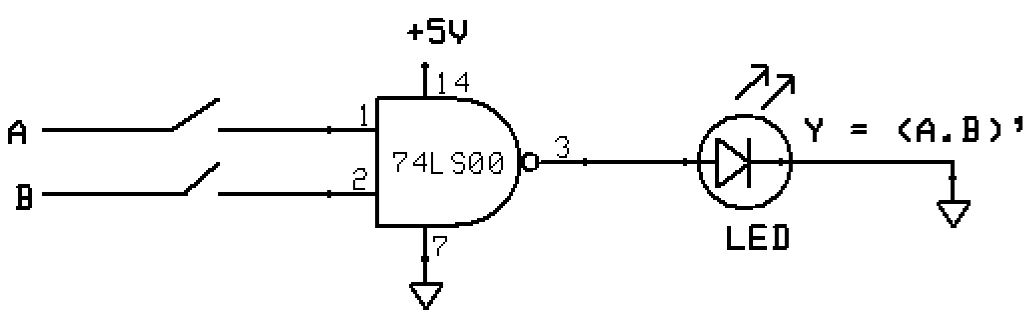
LOGIC DIAGRAM:



PIN DIAGRAM OF IC 7400 :



CIRCUIT DIARAM:



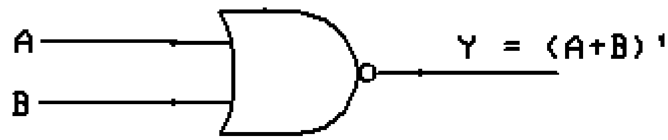
TRUTH TABLE:

S.No	INPUT		OUTPUT
	A	B	Y = (A. B)'
1.	0	0	1
2.	0	1	1

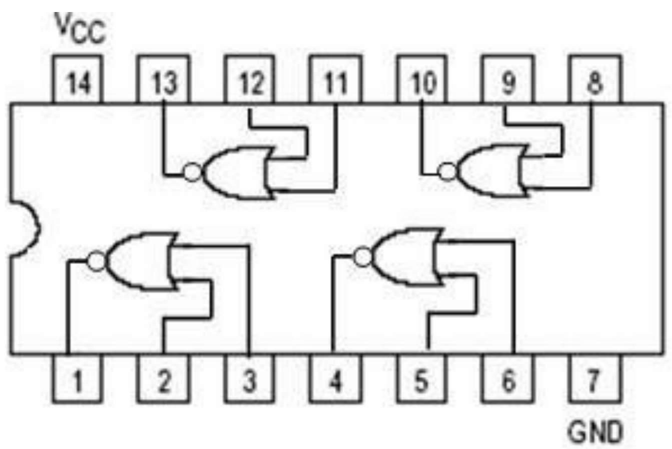
3.	1	0	1
4.	1	1	0

NORGATE

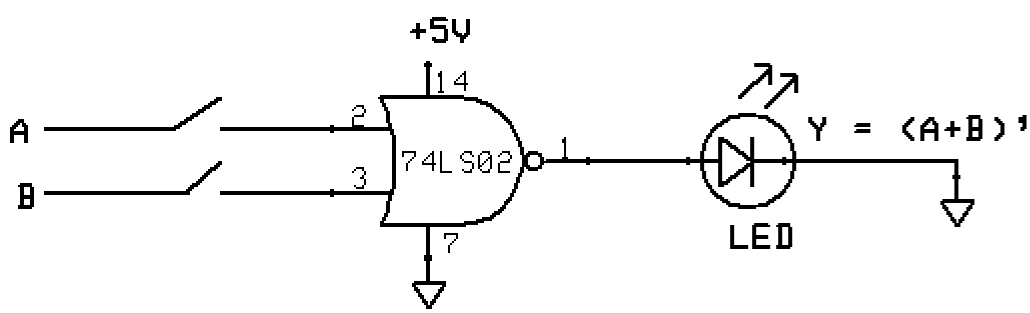
LOGIC DIAGRAM:



PIN DIAGRAM OF IC 7402 :



CIRCUIT DIAGRAM:

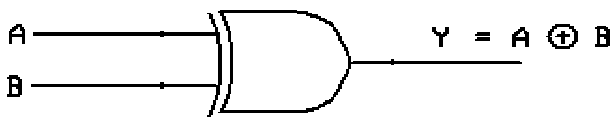


TRUTH TABLE:

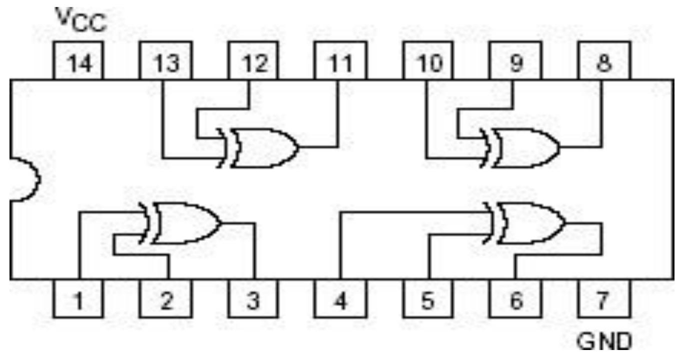
S.No	INPUT		OUTPUT
	A	B	Y = (A + B)'
1.	0	0	1
2.	0	1	0
3.	1	0	0
4.	1	1	0

EX-ORGATE

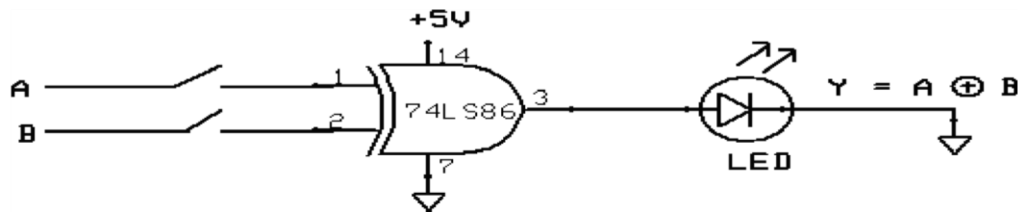
LOGIC DIAGRAM



PIN DIAGRAM OF IC 7486:



CIRCUIT DIAGRAM:



TRUTH TABLE:

S.No	INPUT		OUTPUT
	A	B	$Y = A \oplus B$
1.	0	0	0
2.	0	1	1
3.	1	0	1
4.	1	1	0

DISCUSSION QUESTIONS:

1. What is Integrated Circuit?
2. What is a Logic gate?
3. What are the basic digital logic gates?
4. What are the gates called universal gates?
5. Why NAND and NOR gates are called universal gates?
6. What are the properties of EX-NOR gate?

RESULT:

The truth tables of all the basic digital ICs were verified.

Ex.No

IMPLEMENTATION OF BOOLEAN FUNCTIONS

Date:

AIM:

To design the logic circuit and verify the truth table of the given Boolean expression,
F (A,B,C,D) = Σ (0,1,2,5,8,9,10)

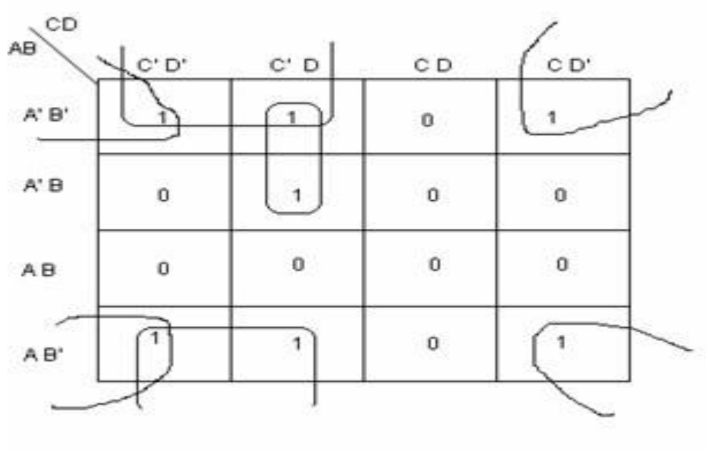
APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	AND gate	IC 7408	1
3.	OR gate	IC 7432	1
4.	NOT gate	IC 7404	1
5.	Connecting wires		As required

DESIGN:

Given , F (A,B,C,D) = Σ (0,1,2,5,8,9,10)

The output function F has four input variables hence a four variable Karnaugh Map is used to obtain a simplified expression for the output as shown,



From the K-Map,

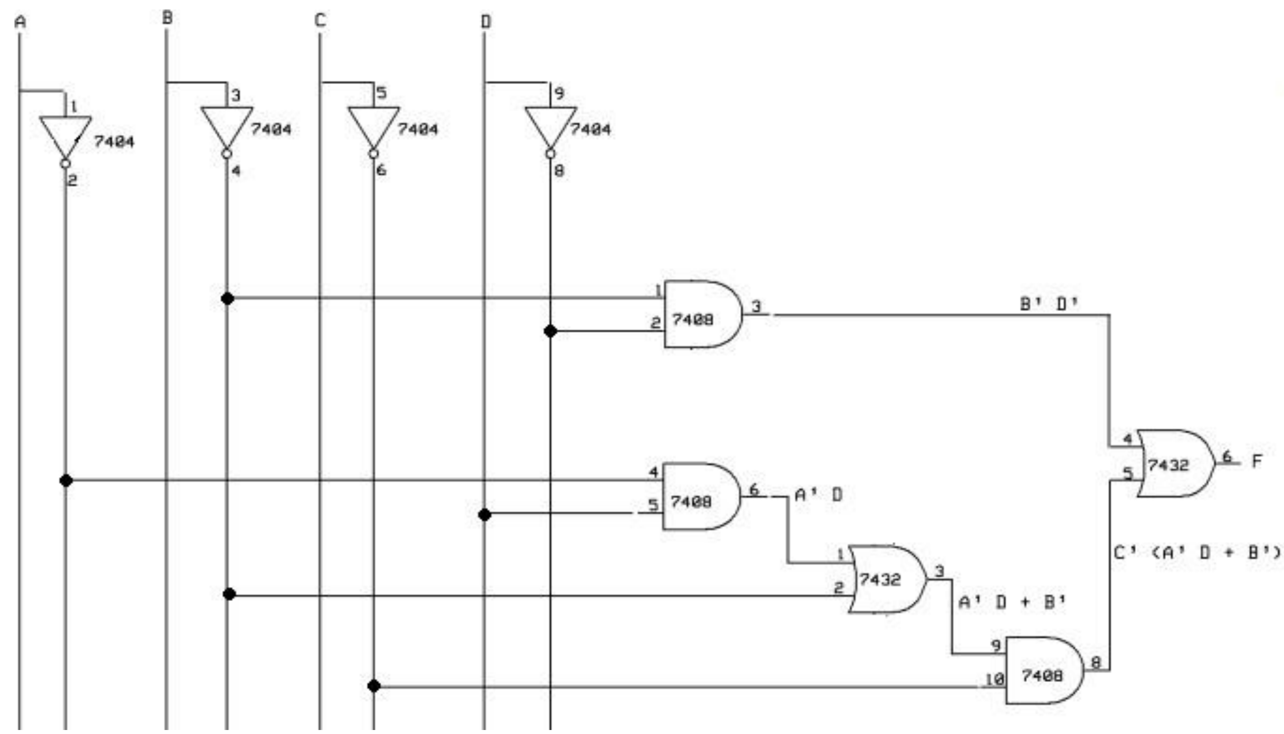
F = B’ C’ + D’ B’ + A’ C’ D

Since we are using only two input logic gates the above expression can be re-written as,

F = C’ (B’ + A’ D) + D’ B’

Now the logic circuit for the above equation can be drawn.

CIRCUIT DIAGRAM:



TRUTH TABLE:

S.No	INPUT				OUTPUT
	A	B	C	D	F=D'B'+C'(B'+A'D)
1.	0	0	0	0	1
2.	0	0	0	1	1
3.	0	0	1	0	1
4.	0	0	1	1	0
5.	0	1	0	0	0
6.	0	1	0	1	1
7.	0	1	1	0	0
8.	0	1	1	1	0
9.	1	0	0	0	1
10.	1	0	0	1	1
11.	1	0	1	0	1
12.	1	0	1	1	0
13.	1	1	0	0	0
14.	1	1	0	1	0
15.	1	1	1	0	0

	16.	1	1	1	1	0	

PROCEDURE:

1. Connections are given as per the circuit diagram
2. For all the ICs 7th pin is grounded and 14th pin is given +5 V supply.
3. Apply the inputs and verify the truth table for the given Boolean expression.

DISCUSSION QUESTIONS:

1. What is variable mapping?
2. Define Demorgans theorem.
3. What do you mean by don't care functions?
4. State two absorption properties of Boolean function.
5. What are the two methods of Boolean function minimization?

RESULT:

The truth table of the given Boolean expression was verified.

Ex.No:

DESIGN AND IMPLEMENTATION OF ADDER/SUBTRACTOR

Date:

AIM:

To design and construct half adder, full adder, half subtractor and full subtractor circuits and verify the truth table using logic gates.

APPARATUS REQUIRED:

S. No	N	Specification	Quantity
1.	IC	7432(OR), 7408(AND), 7486(EX-OR), 7404(NOT)	Each 1
2.	Digital IC Trainer Kit		1
3.	Patch chords		-

THEORY:

The most basic arithmetic operation is the addition of two binary digits. There are four possible elementary operations, namely,

$$0 + 0 = 0$$
$$0 + 1 = 1$$
$$1 + 0 = 1$$
$$1 + 1 = 10$$

The first three operations produce a sum of whose length is one digit, but when the last operation is performed the sum is two digits. The higher significant bit of this result is called a carry and lower significant bit is called the sum.

HALFADDER:

A combinational circuit which performs the addition of two bits is called half adder. The input variables designate the augend and the addend bit, whereas the output variables produce the sum and carry bits.

FULLADDER:

A combinational circuit which performs the arithmetic sum of three input bits is called full adder. The three input bits include two significant bits and a previous carry bit. A full adder circuit can be implemented with two half adders and one OR gate.

HALFADDER

TRUTH TABLE:

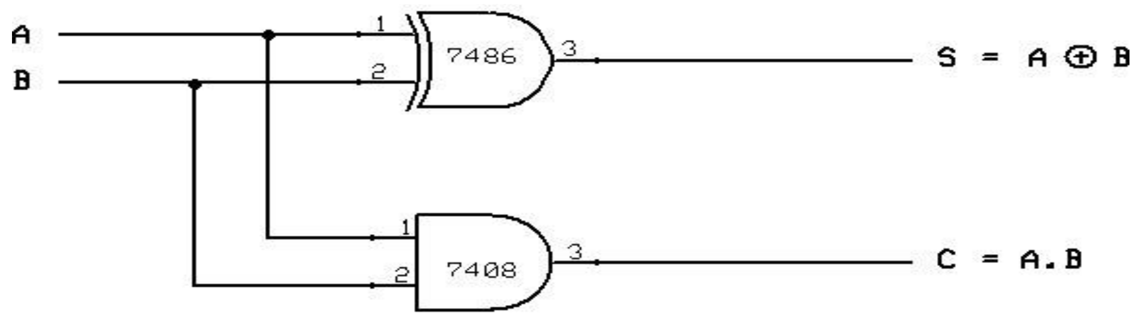
S.No	INPUT		OUTPUT	
	A	B	S	C

1.	0	0	0	0
2.	0	1	1	0
3.	1	0	1	0
4.	1	1	0	1

DESIGN:

From the truth table the expression for sum and carry bits of the output can be obtained as, Sum, S = A ⊕ B ; Carry, C = A . B

CIRCUIT DIAGRAM:



FULL ADDER

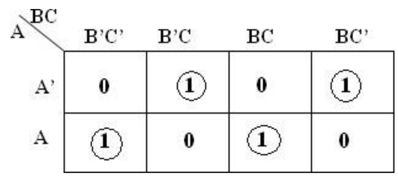
TRUTH TABLE:

S.No	INPUT			OUTPUT	
	A	B	C	SUM	CARRY
1.	0	0	0	0	0
2.	0	0	1	1	0
3.	0	1	0	1	0
4.	0	1	1	0	1
5.	1	0	0	1	0
6.	1	0	1	0	1
7.	1	1	0	0	1
8.	1	1	1	1	1

DESIGN:

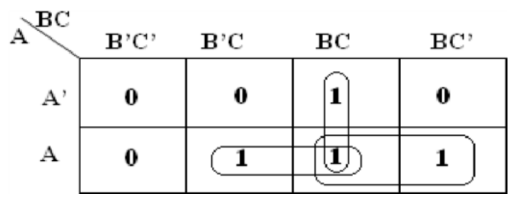
From the truth table the expression for sum and carry bits of the output can be obtained as,SUM = A’B’C + A’BC’ + AB’C’ + ABC;CARRY = A’BC + AB’C + ABC’ +ABC Using Karnaugh maps the reduced expression for the output bits can be obtained as,

<u>SUM</u>



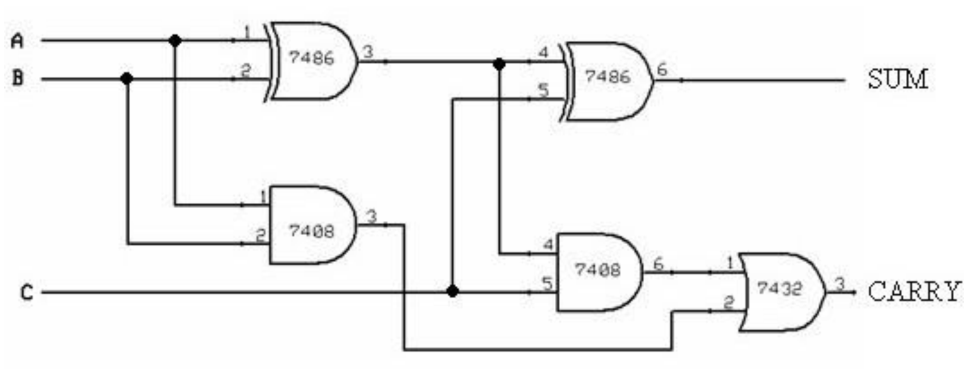
SUM = A’B’C + A’BC’ + AB’C’ + ABC = A $\oplus$ B $\oplus$ C

<u>CARRY</u>



CARRY = AB + AC + BC

CIRCUIT DIAGRAM:



HALF SUBTRACTOR

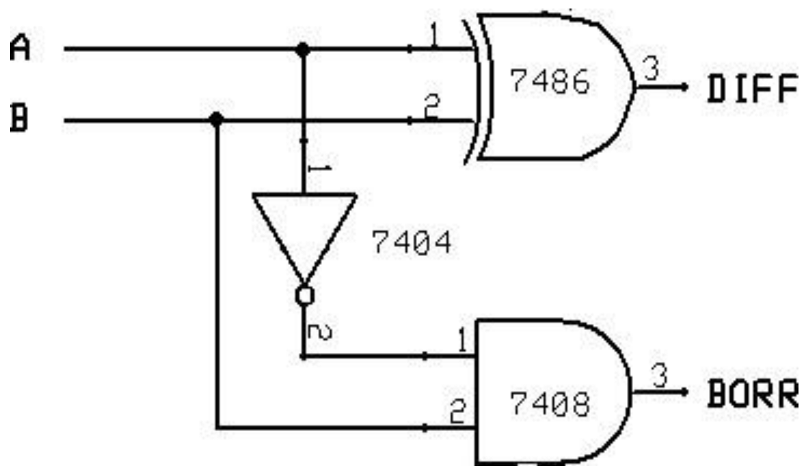
TRUTH TABLE:

S.No	INPUT		OUTPUT	
	A	B	DIFF	BORR
1.	0	0	0	0
2.	0	1	1	1
3.	1	0	1	0
4.	1	1	0	0

DESIGN:

From the truth table the expression for difference and borrow bits of the output can be obtained as, Difference, DIFF = A ⊕ B; Borrow, BORR = A' . B

CIRCUIT DIAGRAM:



FULL SUBTRACTOR TRUTH TABLE:

S.No	INPUT			OUTPUT	
	A	B	C	DIFF	BORR
1.	0	0	0	0	0
2.	0	0	1	1	1
3.	0	1	0	1	1
4.	0	1	1	0	1
5.	1	0	0	1	0
6.	1	0	1	0	0
7.	1	1	0	0	0
8.	1	1	1	1	1

DESIGN:

From the truth table the expression for difference and borrow bits of the output can be obtained as,

Difference, DIFF= A’B’C + A’BC’ + AB’C’ + ABC
Borrow, BORR = A’BC + AB’C + ABC’ +ABC

Using Karnaugh maps the reduced expression for the output bits can be obtained as,

DIFFERENCE

A \ BC	B’C’	B’C	BC	BC’
A’	0	1	0	1
A	1	0	1	0

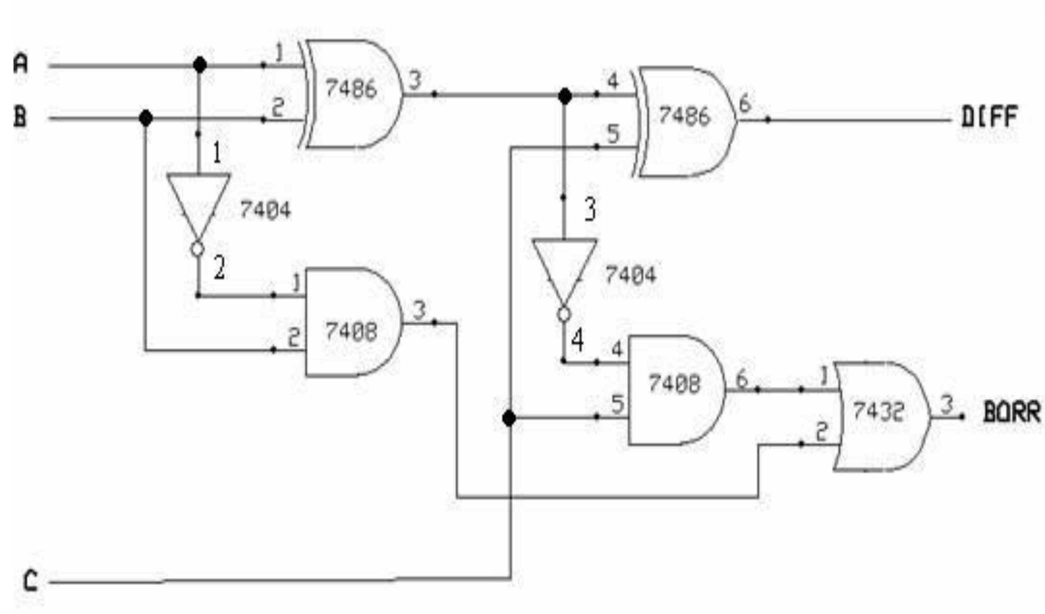
A’B’C + A’BC’ + AB’C’ + ABC = A ⊕ B ⊕ C

BORROW

A \ BC	B’C’	B’C	BC	BC’
A’	0	1	1	1
A	0	0	1	0

BORROW = A’B + A’C + BC

CIRCUIT DIAGRAM:



A
B
C
7486
7486
DIFF
7404
7404
7408
7408
7432
BORR

HALFSUBTRACTOR:

A combinational circuit which performs the subtraction of two bits is called half subtractor. The input variables designate the minuend and the subtrahend bit, whereas the output variables produce the difference and borrow bits.

FULLSUBTRACTOR:

A combinational circuit which performs the subtraction of three input bits is called full subtractor. The three input bits include two significant bits and a previous borrow bit. A full subtractor circuit can be implemented with two half subtractors and one OR gate.

PROCEDURE:

- The connections are given as per the circuit diagram.
- Two 4 – bit numbers added or subtracted depend upon the control input and the output is obtained.
- Apply the inputs and verify the truth table for thehalf adder or s subtractor and full adder or subtractor circuits.

DISCUSSION QUESTIONS:

1. What is a combinational circuit?
2. What is different between combinational and sequential circuit?
3. What are the gates involved for binary adder?
4. List the properties of Ex-Nor gate?
5. What is the expression for sum and carry in half and full adder?

RESULT:

Thus the half adder, full adder, half subtractor and full subtractor circuits were designed and their truth table were verified.

Ex. No:

Date:

PARITY GENERATOR & CHECKER

AIM:

To design and verify the truth table of a three bit Odd Parity generator and checker & Even Parity Generator And Checker.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	EX-OR gate	IC 7486	1
3.	NOT gate	IC 7404	1
4.	Connecting wires		As required

THEORY:

A parity bit is used for the purpose of detecting errors during transmission of binary information. A parity bit is an extra bit included with a binary message to make the number of 1's either odd or even. The message including the parity bit is transmitted and then checked at the receiving end for errors. An error is detected if the checked parity does not correspond with the one transmitted. The circuit that generates the parity bit in the transmitter is called a parity generator and the circuit that checks the parity in the receiver is called a parity checker.

In even parity the added parity bit will make the total number of 1's an even amount and in odd parity the added parity bit will make the total number of 1's an odd amount.
In a three bit odd parity generator the three bits in the message together with the parity bit are transmitted to their destination, where they are applied to the parity checker circuit. The parity checker circuit checks for possible errors in the transmission.

Since the information was transmitted with odd parity the four bits received must have an odd number of 1's. An error occurs during the transmission if the four bits received have an even number of 1's, indicating that one bit has changed during transmission. The output of the parity checker is denoted by PEC (parity error check) and it will be equal to 1 if an error occurs, i.e., if the four bits received has an even number of 1's.

PARITYGENERATOR

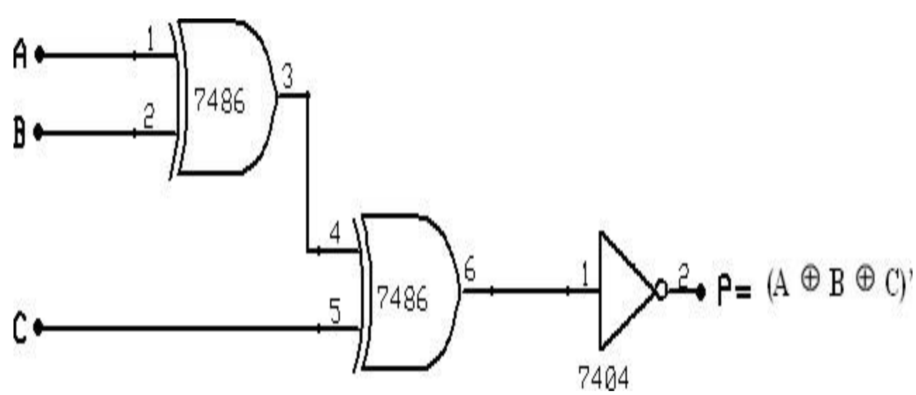
TRUTH TABLE:

S.No	INPUT (Three bit message)			OUTPUT (Odd Parity bit)	OUTPUT (Even Parity bit)
	A	B	C	P	P
1.	0	0	0	1	0
2.	0	0	1	0	1
3.	0	1	0	0	1
4.	0	1	1	1	0
5.	1	0	0	0	1
6.	1	0	1	1	0
7.	1	1	0	1	0
8.	1	1	1	0	1

From the truth table the expression for the output parity bit is, $P(A, B, C) = \Sigma (0, 3, 5, 6)$
Also written as, $P = A'B'C' + A'BC + AB'C + ABC' = (A \oplus B \oplus C)'$

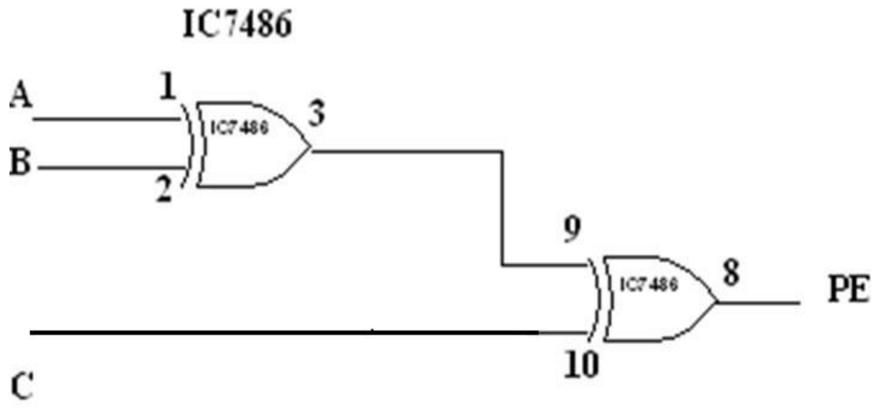
CIRCUIT DIAGRAM:

ODD PARITY GENERATOR

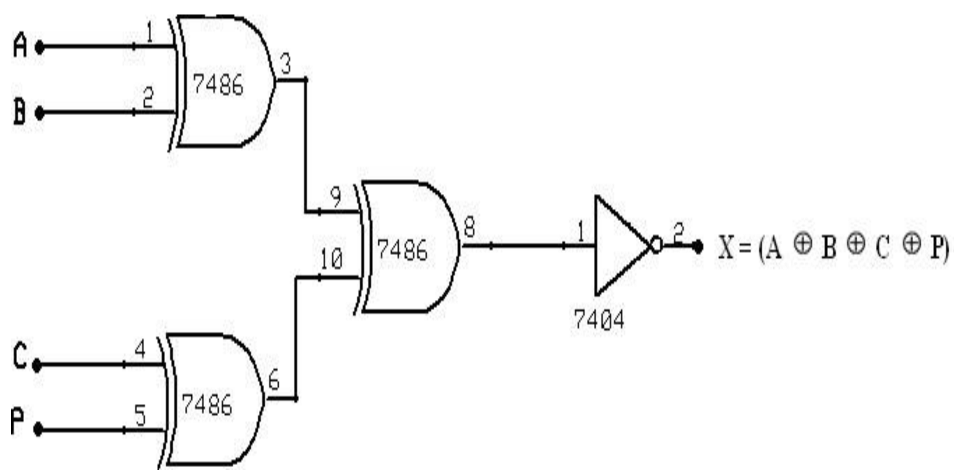


CIRCUIT DIAGRAM:

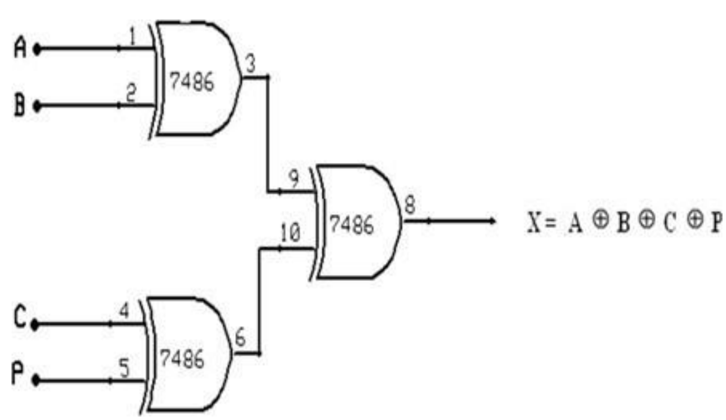
EVENPARITYGENERATOR



ODD PARITYCHECKER



EVEN PARITYCHECKER



PROCEDURE:

1. Connections are given as per the circuit diagrams.

2. For all the ICs 7th pin is grounded and 14th pin is given +5 V supply.
3. Apply the inputs and verify the truth table for the Parity generator and checker.

DISCUSSION QUESTIONS:

1. What is parity bit?
2. Why parity bit is added to message?
3. What is parity checker?
4. What is odd parity and even parity?
5. What are the gates involved for parity generator?

RESULT:

The design of the three bit odd Parity generator and checker& Even Parity Generator and Checker circuits was done and their truth tables were verified.

Ex. No: Date:

CODE CONVERTER

AIM:

To construct and verify the performance of binary to gray and gray to binary.

APPARATUS REQUIRED:

S. No	N	Specification	Quantity
1.	IC	7404(NOT), 7486(EX-OR), 7408(AND), 7432(OR)	Each 1
2.	Digital IC Trainer Kit		1
3.	Connecting wires		-

THEORY:

BINARY TO GRAY:

The MSB of the binary code alone remains unchanged in the Gray code. The remaining bits in the gray are obtained by EX-OR ing the corresponding gray code bit and previous bit in the binary code. The gray code is often used in digital systems because it has the advantage that only one bit in the numerical representation changes between successive numbers.

GRAY TO BINARY**:**

The MSB of the Gray code remains unchanged in the binary code the remaining bits are obtained by EX – OR ing the corresponding gray code bit and the previous output binary bit.

PROCEDURE:

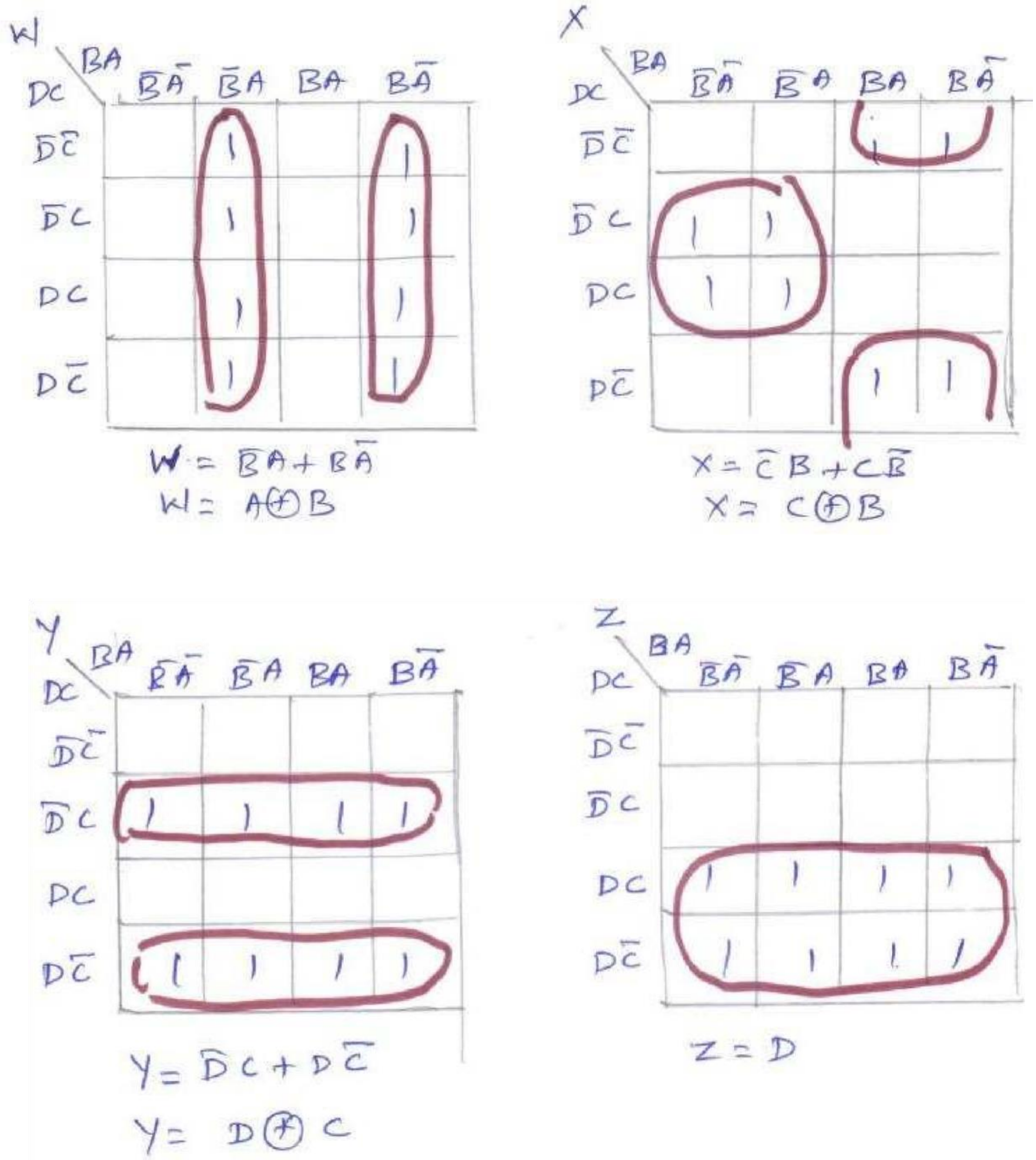
- Connections are given as per the logic diagram.
- The given truth tables are verified.

BINARY TOGRAY:

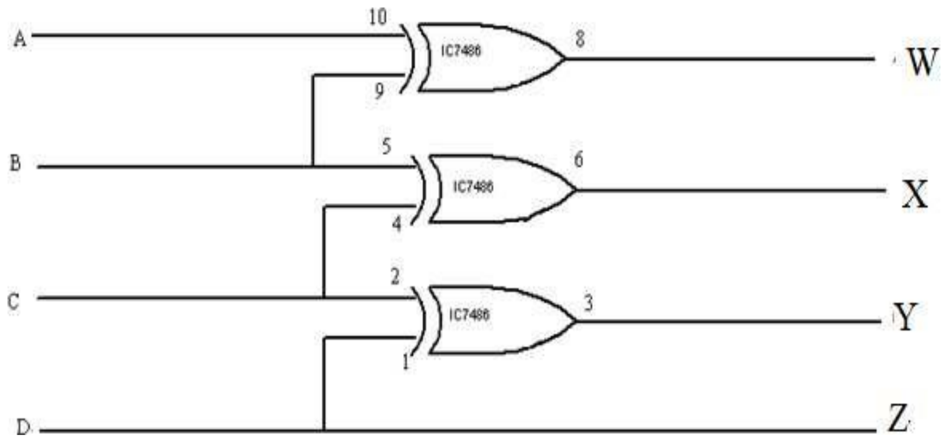
TRUTH TABLE

Decimal	Binary code				Gray code			
	D	C	B	A	Z	Y	X	W
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

K-map design



Logic diagram



GRAY TO BINARY

TRUTH TABLE

Decimal	Gray code				Binary code			
	Z	Y	X	W	D	C	B	A
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
3	0	0	1	1	0	0	1	0
2	0	0	1	0	0	0	1	1
6	0	1	1	0	0	1	0	0
7	0	1	1	1	0	1	0	1
5	0	1	0	1	0	1	1	0
4	0	1	0	0	0	1	1	1
12	1	1	0	0	1	0	0	0
13	1	1	0	1	1	0	0	1
15	1	1	1	1	1	0	1	0
14	1	1	1	0	1	0	1	1
10	1	0	1	0	1	1	0	0
11	1	0	1	1	1	1	0	1
9	1	0	0	1	1	1	1	0
8	1	0	0	0	1	1	1	1

K-Map Design

D

zy \ xw	$\bar{x}w$	$\bar{x}w$	xw	$x\bar{w}$
$\bar{z}\bar{y}$				
$\bar{z}y$				
zy	1	1	1	1
$z\bar{y}$	1	1	1	1

$$D = z$$

C

zy \ xw	$\bar{x}\bar{w}$	$\bar{x}w$	xw	$x\bar{w}$
$\bar{z}\bar{y}$				
$\bar{z}y$	1	1	1	1
zy				
$z\bar{y}$	1	1	1	1

$$C = \bar{z}y + z\bar{y}$$

$$C = z \oplus y$$

B

zy \ xw	$\bar{x}\bar{w}$	$\bar{x}w$	xw	$x\bar{w}$
$\bar{z}\bar{y}$			1	1
$\bar{z}y$	1	1		
zy			1	1
$z\bar{y}$	1	1		

$$B = \bar{z}\bar{y}x + \bar{z}y\bar{x} + zyx + z\bar{y}\bar{x}$$

$$= (\bar{z}y + z\bar{y})\bar{x} + (\bar{z}\bar{y} + zy)x$$

$$= C\bar{x} + \bar{C}x = C \oplus x$$

$$A = \bar{z}\bar{y}\bar{x}w + \bar{z}\bar{y}x\bar{w} + \bar{z}y\bar{x}\bar{w} + \bar{z}yxw + zy\bar{x}w + zyx\bar{w} + z\bar{y}\bar{x}\bar{w} + z\bar{y}xw$$

A

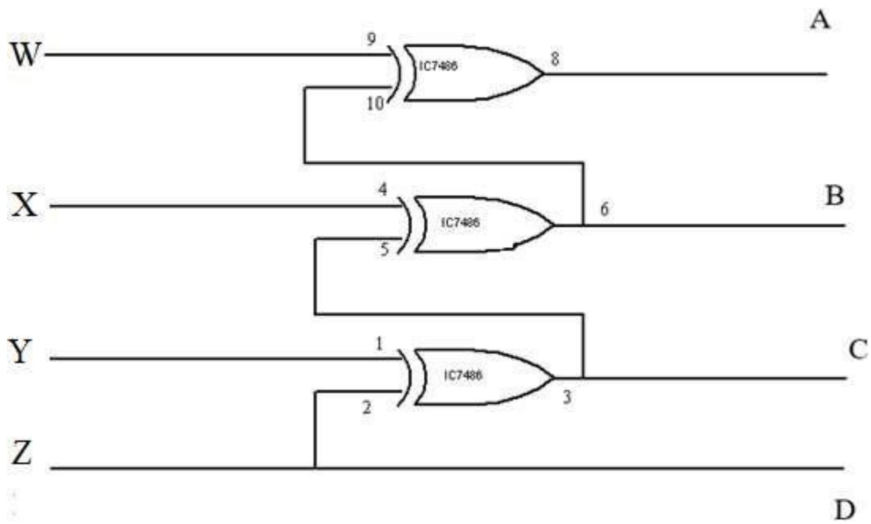
zy \ xw	$\bar{x}\bar{w}$	$\bar{x}w$	xw	$x\bar{w}$
$\bar{z}\bar{y}$	0	1	0	1
$\bar{z}y$	1	0	1	0
zy	0	1	0	1
$z\bar{y}$	1	0	1	0

$$A = (\bar{z}\bar{y}\bar{x} + \bar{z}yx + zy\bar{x} + \bar{z}yx)w + (\bar{z}\bar{y}x + \bar{z}y\bar{x} + zyx + z\bar{y}\bar{x})\bar{w}$$

$$= \bar{B}w + B\bar{w}$$

$$A = B \oplus w$$

Logic Diagram

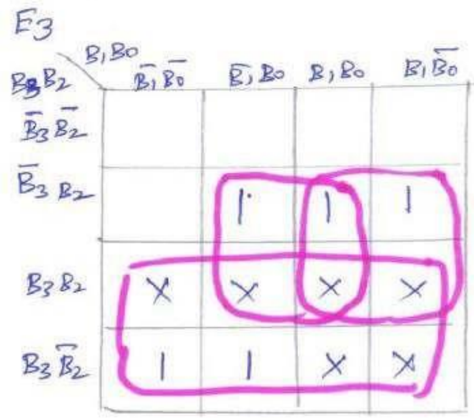


BCD TO EXCESS-3

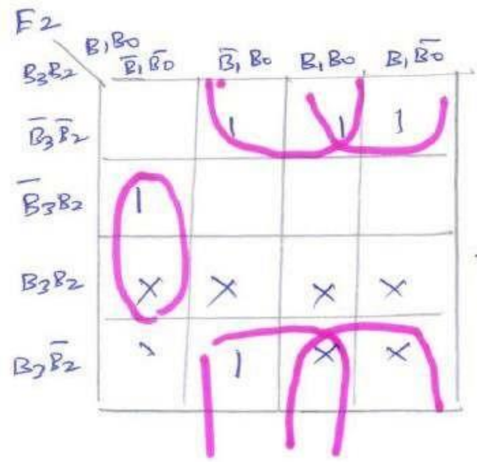
BCD Input				Excess-3 Output			
B3	B2	B1	B0	E3	E2	E1	E0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	×	×	×	×
1	0	1	1	×	×	×	×
1	1	0	0	×	×	×	×
1	1	0	1	×	×	×	×
1	1	1	0	×	×	×	×
1	1	1	1	×	×	×	×

TRUTH TABLE

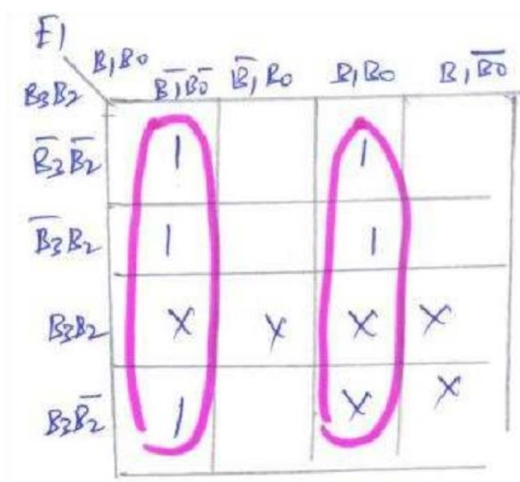
K-Map design



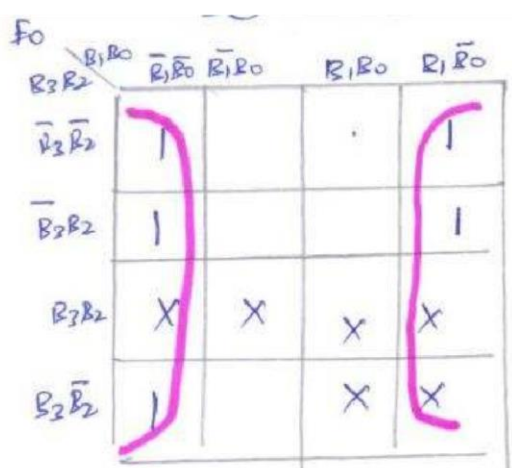
$$E_3 = B_3 + B_2 B_0 + B_2 B_1$$
$$= B_3 + B_2 (B_1 + B_0)$$



$$E_2 = \overline{B_2} B_0 + \overline{B_2} B_1 + B_2 \overline{B_1} \overline{B_0}$$
$$= \overline{B_2} (B_0 + B_1) + B_2 \overline{B_1} \overline{B_0}$$
$$= \overline{B_2} (B_0 + B_1) + B_2 (\overline{B_0 + B_1})$$
$$= B_2 \oplus (B_0 + B_1)$$

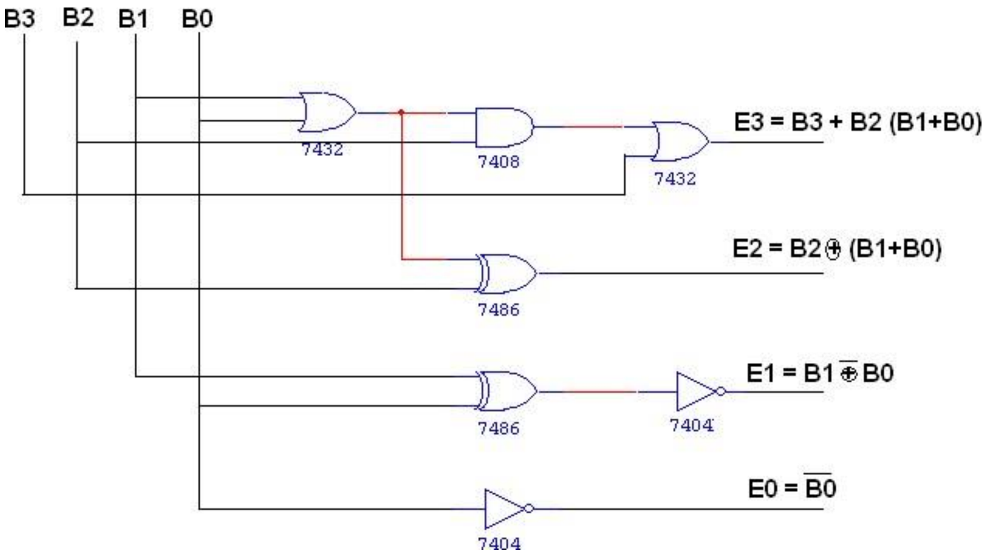


$$E_1 = \overline{B_1} \overline{B_0} + B_1 B_0$$
$$= \overline{B_1 \oplus B_0}$$



$$E_0 = \overline{B_0}$$

Logic diagram

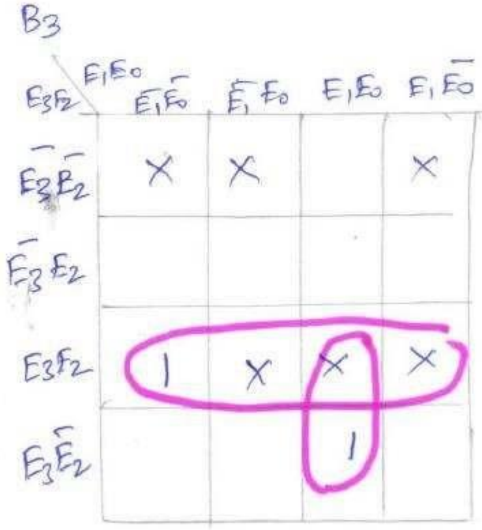


EXCESS-3 TO BCD

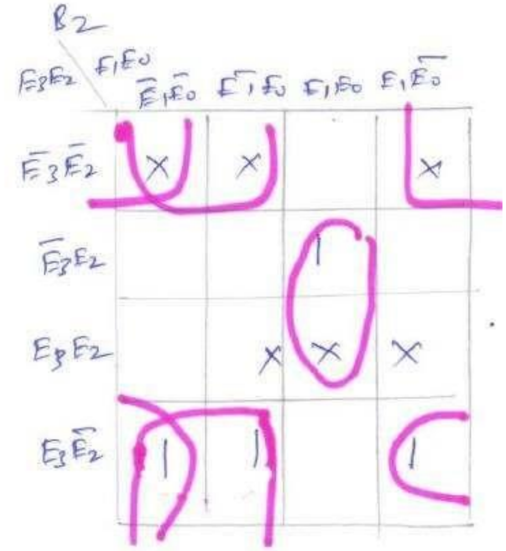
TRUTH TABLE

Excess-3 Input				BCD Output			
E3	E2	E1	E0	B3	B2	B1	B0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1

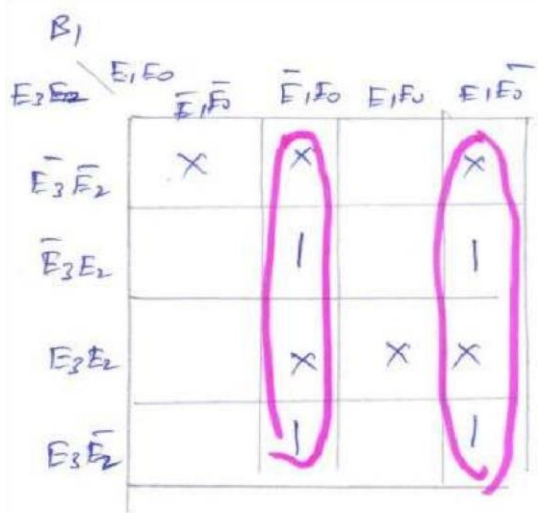
K-map design



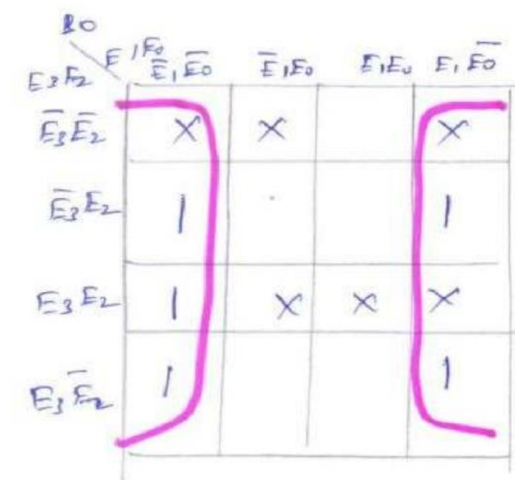
$$B_3 = E_3E_2 + E_3E_1E_0$$
$$= E_3(E_2 + E_1E_0)$$



$$B_2 = \bar{E_2}\bar{E_0} + E_2E_1E_0 + \bar{E_2}\bar{E_1}$$
$$= \bar{E_2}(\bar{E_0} + \bar{E_1}) + E_2(E_1E_0)$$
$$= E_2 \oplus (\bar{E_1} + \bar{E_0})$$

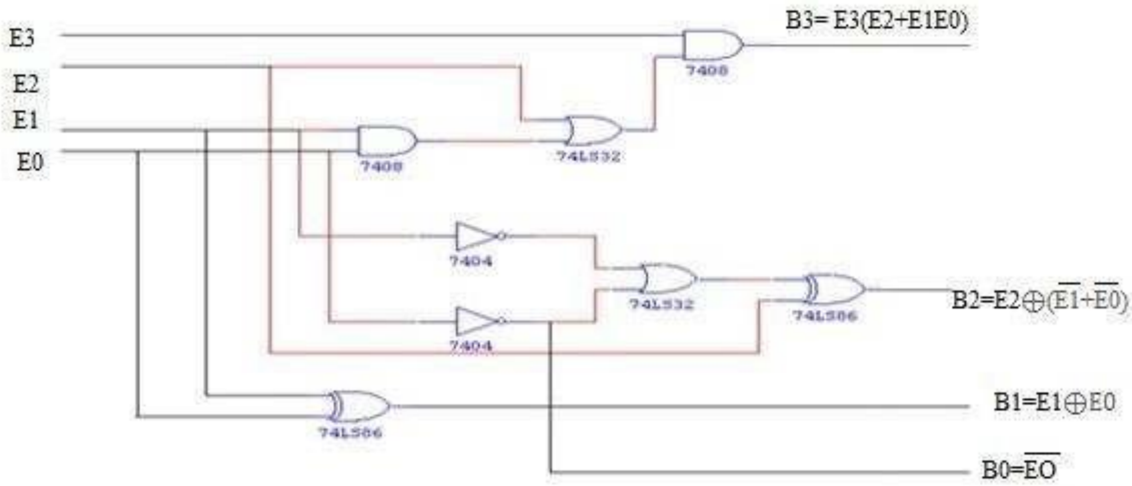


$$B_1 = \bar{E_1}E_0 + E_1\bar{E_0}$$
$$= E_1 \oplus E_0$$



$$B_0 = \bar{E_0}$$

Logic diagram



DISCUSSION QUESTIONS:

1. List the procedures to convert gray code into binary?
2. Why weighted code is called as reflective codes?
3. What is a sequential code?
4. What is error deducting code?
5. What is ASCII code?

RESULT:

The design of the three bit Binary to Gray code converter & Vice versa and BCD to Excess-3 code converter & Vice versa were done and its truth table were verified.

Ex. No: **ENCODER & DECODER**

Date:

AIM:

To design and implement encoder and decoder using logic gates

APPARATUS REQUIRED:

S. No	N	Specification	Quantity
1.	IC	7432(OR)	3
2.	IC	7408(AND), 7404(NOT)	Each 1
3.	Digital IC Trainer Kit		1
4.	Patch chords		-

THEORY:

An encoder is digital circuit that has 2^n input lines and n output lines. The output lines generate a binary code corresponding to the input values 8 – 3 encoder circuit has 8 inputs, one for each of the octal digits and three outputs that generate the corresponding binary number. Enable inputs E_1 should be connected to ground and E_o should be connected to V_{CC}

A decoder is a combinational circuit that converts binary information from n input lines to 2n unique output lines. In 2-4 line decoder the three inputs are decoded into right outputs in which each output representing one of the minterm of 2 input variables.

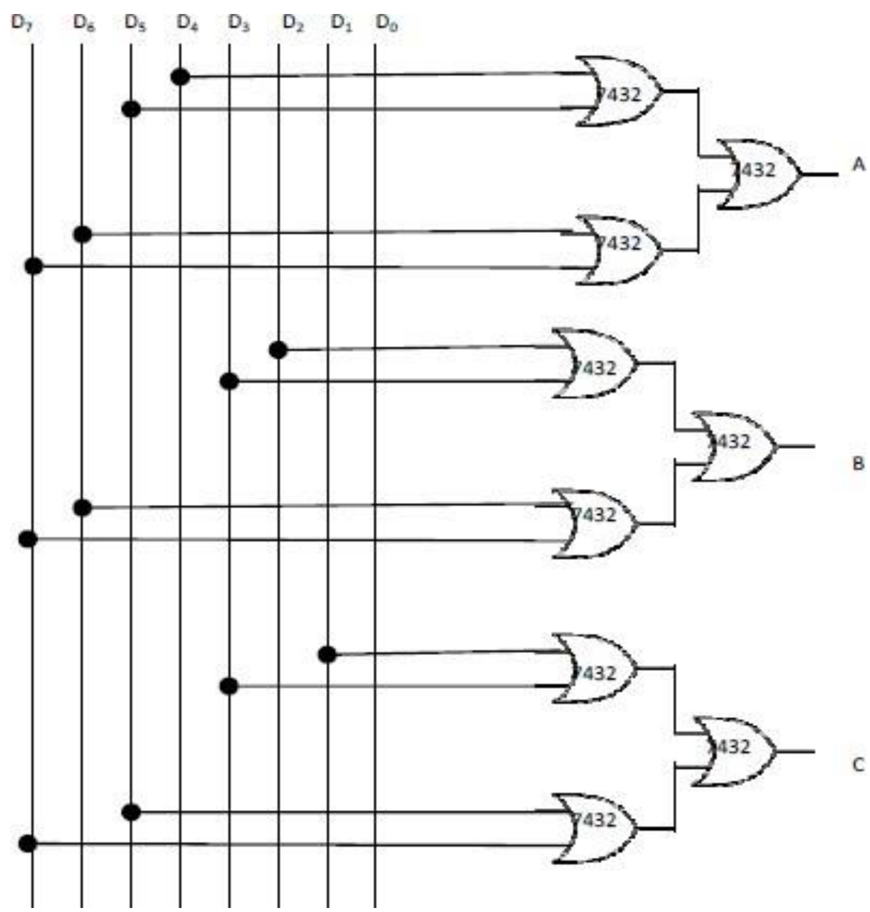
PROCEDURE:

- Connections are given as per the logic diagram.
- The truth table is verified by varying the inputs.

ENCODER
TRUTH TABLE

Input								Output		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A	B	C
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

LOGIC DIAGRAM:

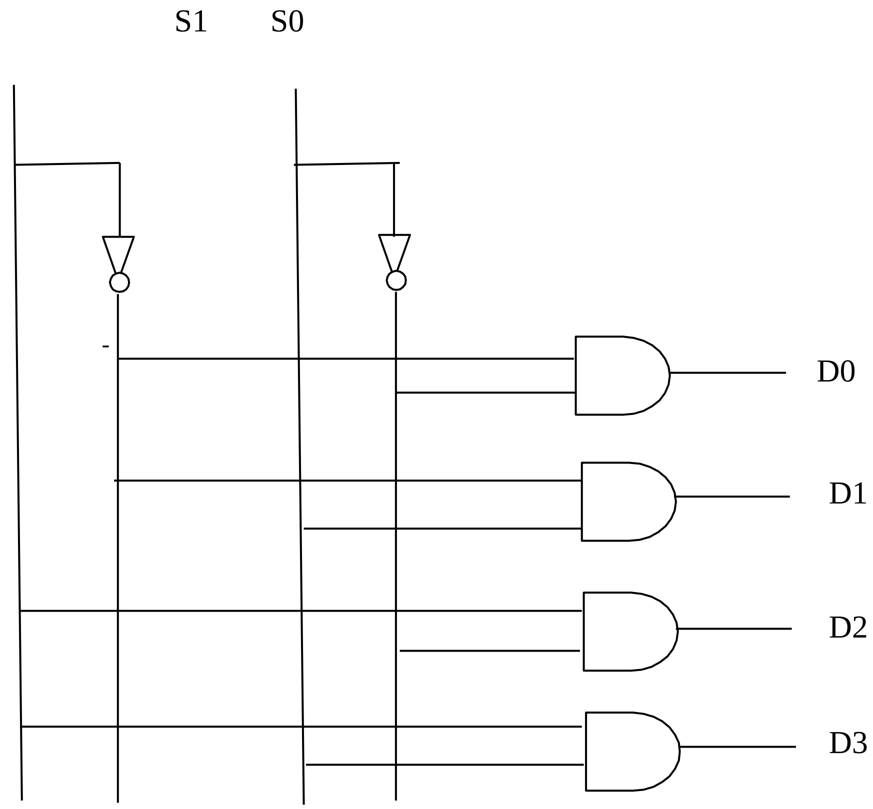


DECODER

TRUTH TABLE

INPUT		OUTPUT			
S1	**S0**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

LOGIC DIAGRAM:



DISCUSSION QUESTIONS:

1. How the output line will be activated in decoder circuit?
2. What are the necessary steps for implementing higher order decoders?
3. What is the use of code converters?
4. How to convert BCD to Decimal decoder?
5. What is seven segment displays?
6. What is the other name of encoder?
7. What is encoding?
8. What are the applications of encoder?
9. What is BCD encoder?

RESULT:

Thus the encoder and decoder circuits were designed and implemented.

Ex. No:
Date: **MULTIPLEXER & DEMULTIPLEXER**

AIM:

To study the truth table of a 4X1 Multiplexer & 1X4 Demultiplexer.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	OR gate	IC 7432	1
3.	NOT gate	IC 7404	1
4.	AND gate (three input)	IC 7411	2
5.	Connecting wires		As required

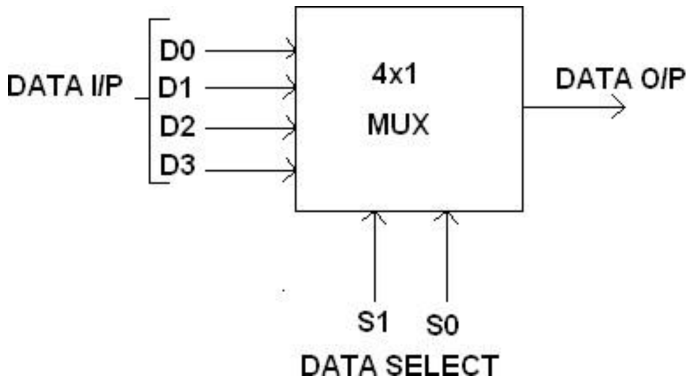
THEORY:

Multiplexer is a digital switch which allows digital information from several sources to be routed onto a single output line. The basic multiplexer has several data input lines and a single output line. The selection of a particular input line is controlled by a set of selection lines.

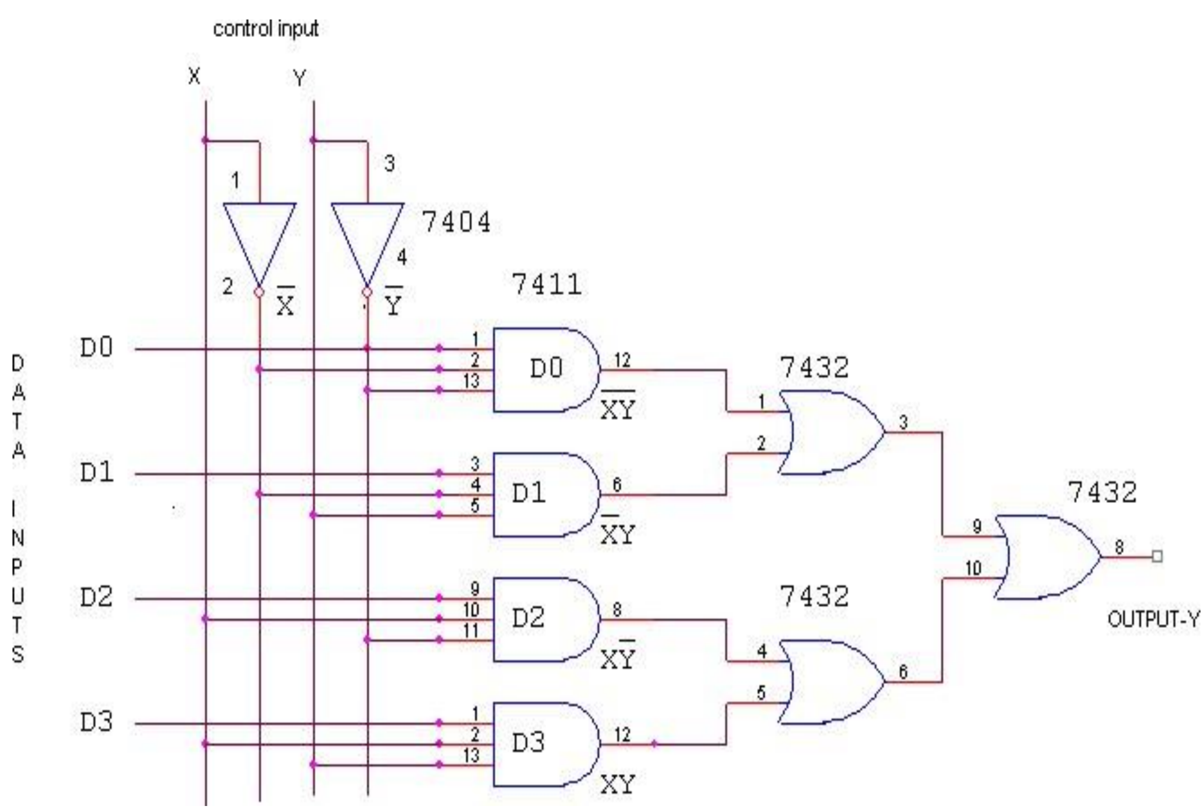
Normally, there are 2^n input lines and n selector lines whose bit combinations determine which input is selected. Therefore, multiplexer is 'many into one' and it provides the digital equivalent of an analog selector switch.

A Demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines. The selection of specific output line is controlled by the values of n selection lines.

BLOCK DIAGRAM FOR 4:1 MULTIPLEXER:



CIRCUIT DIAGRAM : (4 x 1)



FUNCTION TABLE(4 x 1)

X	Y	OUTPUTS (Y)
0	**0**	**D0 → D0 X’ Y’**
0	**1**	**D1 → D1 X’ Y**
1	**0**	**D2 → D2 X Y’**
1	**1**	**D3 → D3 X Y**

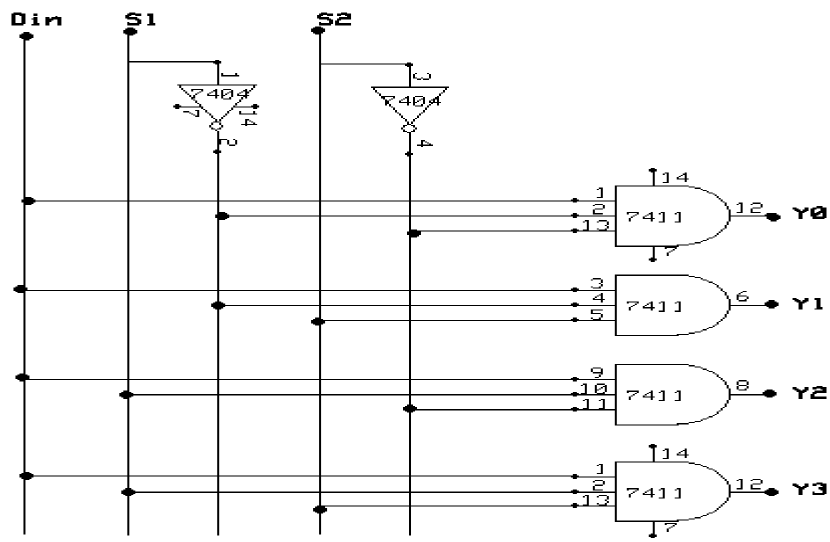
Y = D0 X’ Y’ + D1 X’ Y + D2 X Y’ + D3 X Y

1X4 DEMULTIPLEXER

TRUTH TABLE:

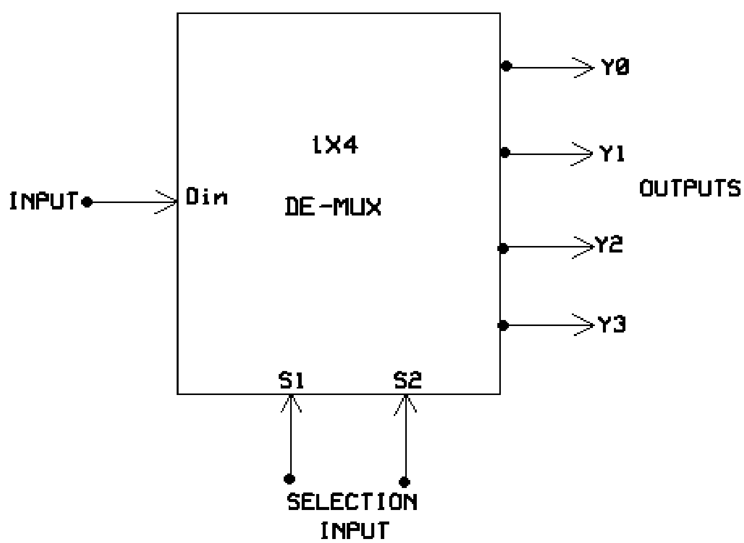
S.No	INPUT			OUTPUT			
	S1	S2	Din	Y0	Y1	Y2	Y3
1.	0	0	0	0	0	0	0
2.	0	0	1	1	0	0	0
3.	0	1	0	0	0	0	0
4.	0	1	1	0	1	0	0
5.	1	0	0	0	0	0	0
6.	1	0	1	0	0	1	0
7.	1	1	0	0	0	0	0
8.	1	1	1	0	0	0	1

CIRCUIT DIAGRAM:



1X4 DEMULTIPLEXER

LOGIC SYMBOL:



PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. For all the ICs 7th pin is grounded and 14th pin is given +5 V supply.
3. Apply the inputs and verify the truth table for the multiplexer & demultiplexer.

DISCUSSION QUESTIONS:

1. What is the other name of de-multiplexer?
2. Compare MUX and DE-MUX?

3. How many select lines needed for four outputs of DE-MUX?
4. What is other name of multiplexer?
5. What is serial to parallel converter?
6. What is the use of select lines?
7. How to enable the multiplexer?
8. What are the applications of multiplexer?

RESULT:

The design of the 4x1 Multiplexer and 1x4 Demultiplexer circuits was done and their truth tables were verified.

Ex. No:

Date:

SHIFT REGISTERS

AIM:

To implement the following shift register using flip flop

(i) SIPO (ii) SISO (iii) PISO (iv) PIPO

APPARATUS REQUIRED:

S. No	Name	Specification	Quantity
1.	IC	7474	2
2.	Digital IC Trainer Kit		1
3.	Connecting wires		-
4	IC	7432 (OR)	1

THEORY:

A register is used to move digital data. A shift register is a memory in which information is shifted from one position in to another position at a line when one clock pulse is applied. The data can be shifted either left or right direction towards right or towards left.

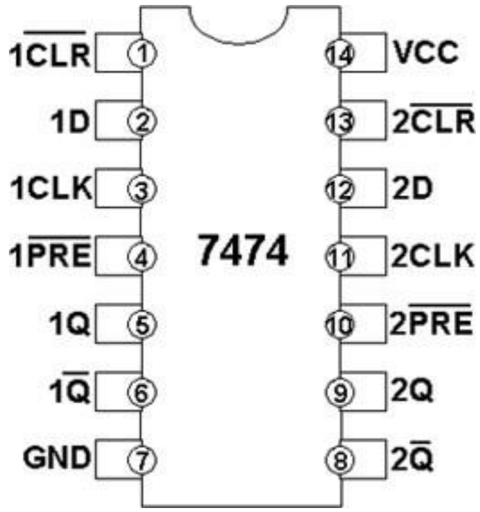
A shift register can be used in four ways depending upon the input in which the data are entered in to and takes out of it. The four configuration are given as

- Serial input – Serial output (SISO)
- Parallel input – Serial output (PISO)
- Serial input – Parallel output (SIPO)
- Parallel input – Parallel output (PIPO) D flip flop is used for constructing shift register.

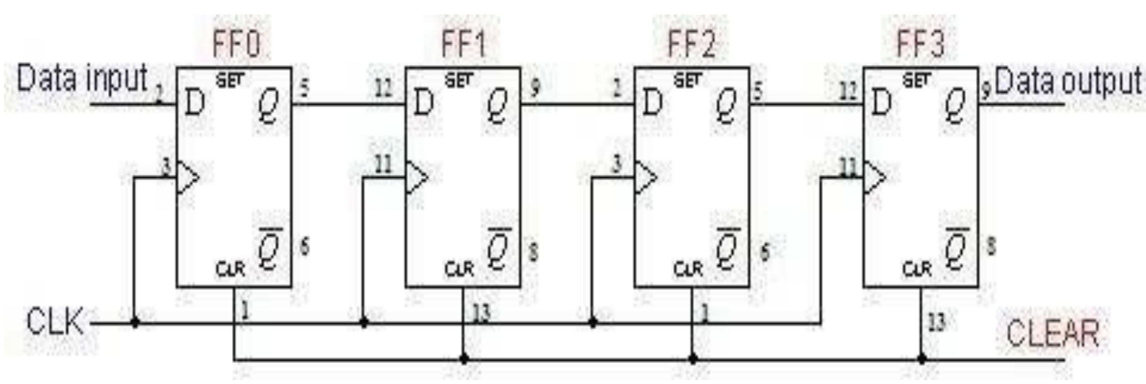
PROCEDURE:

1. Give the connections as per the circuit
2. Set or Reset at the pin 2 which it's the MSB of serial data.
3. Apply a single clock Set or Reset second digital input at pin 2.
4. Repeat step 2 until all 4-bit data are taken away.

D Flip flop IC 7474 - Pin diagram



SHIFT REGISTER: SISO:



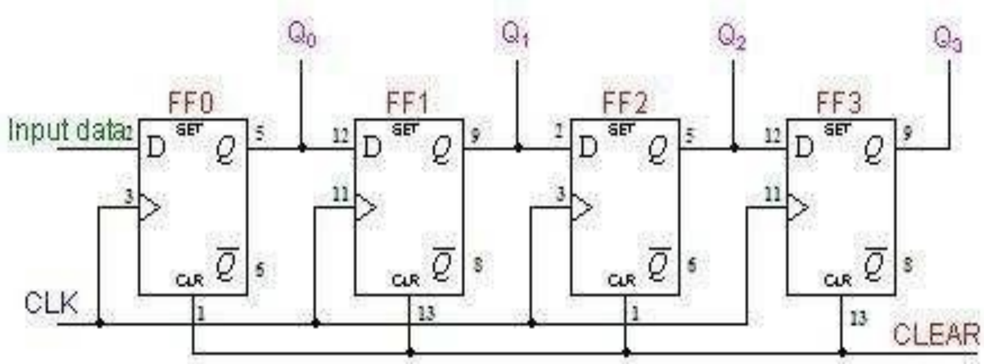
Truth table:

Data input = 1001

Clock	Serial input	Serial output
1	1	0
2	0	0
3	0	0
4	1	1

5	X	0
6	X	0
7	X	1

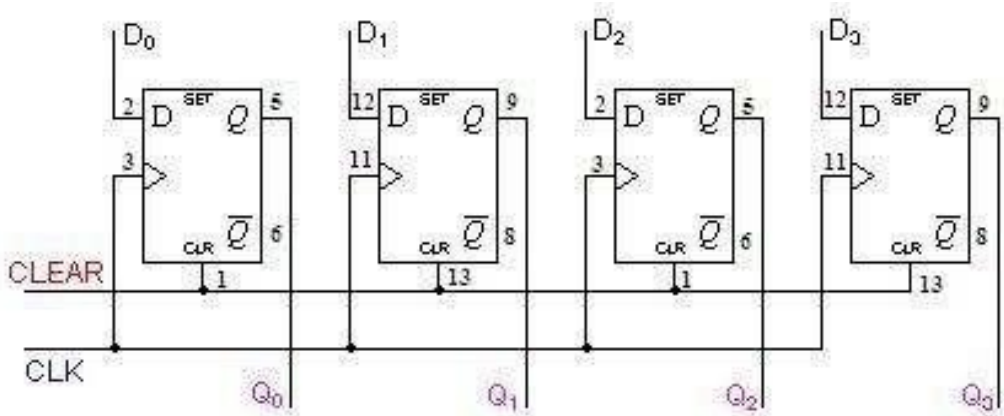
SIPO:



Truth table

No of clk pulse	Serial input D_{in}	Parallel output			
		Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0
1	1	0	0	0	1
2	1	0	0	1	1
3	0	0	1	1	0
4	1	1	1	0	1
5	0	1	0	1	0
6	0	0	1	0	0
7	0	1	0	0	0
8	0	0	0	0	0

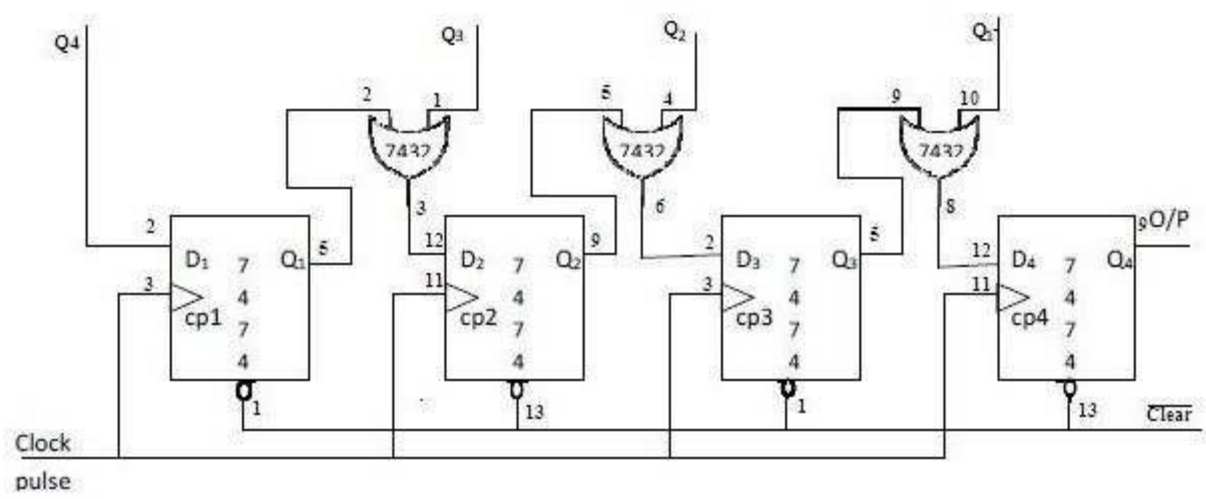
PIPO



Truth table (PIPO)

Clock	Parallel input				Parallel output			
	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0	0	0	0	0
1	1	1	0	1	1	1	0	1

PISO



Truth table

Clock	PARALLEL INPUT				OUTPUT
	Q_4	Q_3	Q_2	Q_1	
1	1	0	0	1	1
2	X	X	X	X	0
3	X	X	X	X	0
4	X	X	X	X	1

DISCUSSION QUESTIONS:

1. What is register?
2. What are the modes of shift register?
3. How ring counter is implemented using shift registers?
4. Compare parallel and serial sub registers?

5. Define sequence generator?
6. What are the types of shift register?
7. Define shift registers.

RESULT:

Thus the SISO, SIPO, PISO, PIPO shift registers were designed and implemented.

Ex. No:

Date: **ASYNCHRONOUS COUNTER**

AIM:

To implement and verify the truth table of an asynchronous counter.

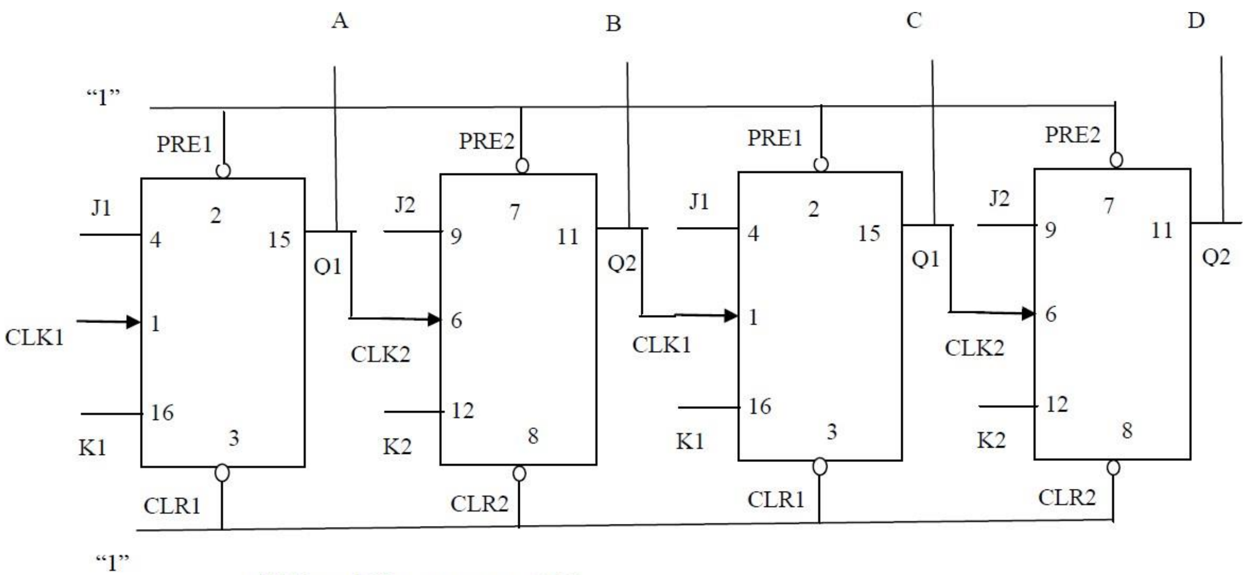
APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	JK Flip Flop	IC 7476	2
3.	Connecting wires		As required

THEORY:

Asynchronous counter is also called as ripple counter. In a ripple counter the flip flop output transition serves as a source for triggering other flip flops. In other words the clock pulse inputs of all the flip flops are triggered not by the incoming pulses but rather by the transition that occurs in other flip flops. The term asynchronous refers to the events that do not occur at the same time. With respect to the counter operation, asynchronous means that the flip flop within the counter are not made to change states at exactly the same time, they do not because the clock pulses are not connected directly to the clock input of each flip flop in the counter.

CIRCUIT DIAGRAM: (4-Bit Asynchronous counter using IC 7476 JK Flip Flop)

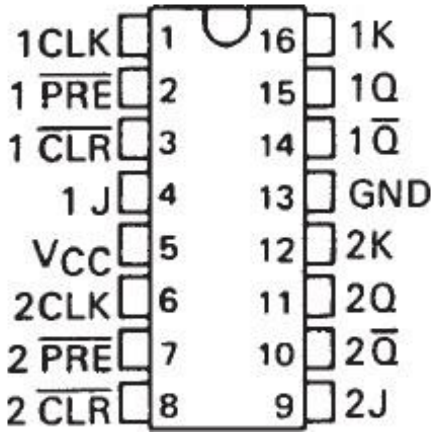


All J and K connect to "1"
1 means logic high or +5V

TRUTH TABLE:

S.No	CLOCK PULSE	OUTPUT			
		D(MSB)	C	B	A(LSB)
1	0	0	0	0	0
2	1	0	0	0	1
3	2	0	0	1	0
4	3	0	0	1	1
5	4	0	1	0	0
6	5	0	1	0	1
7	6	0	1	1	0
8	7	0	1	1	1
9	8	1	0	0	0
10	9	1	0	0	1
11	10	1	0	1	0
12	11	1	0	1	1
13	12	1	1	0	0
14	13	1	1	0	1
14	14	1	1	1	0
16	15	1	1	1	1

JK Flip Flop IC7476 PIN DIAGRAM



PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. Apply the input and verify the truth table of the counter.

Ex. No: Date:

AIM: **SYNCHRONOUS COUNTER**

To design and implement 4-bit synchronous BCD counter.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	JK Flip Flop	IC 7476	2
3.	AND gate	IC 7408	2
	Connecting wires		As required

THEORY:

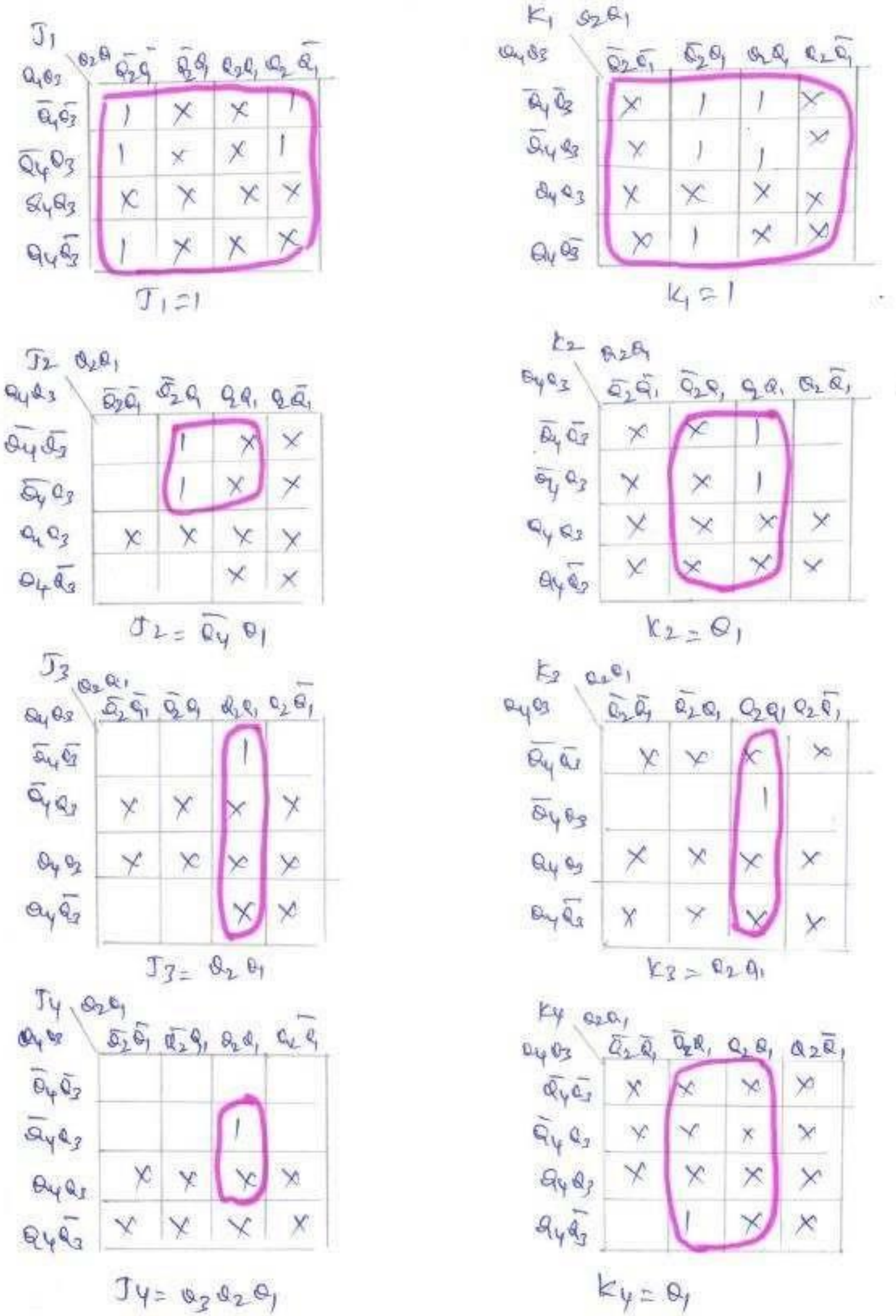
A counter is a register capable of counting number of clock pulse arriving at the clock input. In synchronous counter all the flip-flops are clocked simultaneously .It is faster in speed because of the propagation delay of the single flip-flop is involved. It is also called as a parallel counter. A BCD synchronous counter can be called as a decade counter or mod-10 counter. It requires 4 flip flops ($10<=2^4$). So there are 16 possible states out of which 10 are valid and other 6 are invalid.

TRUTH TABLE:

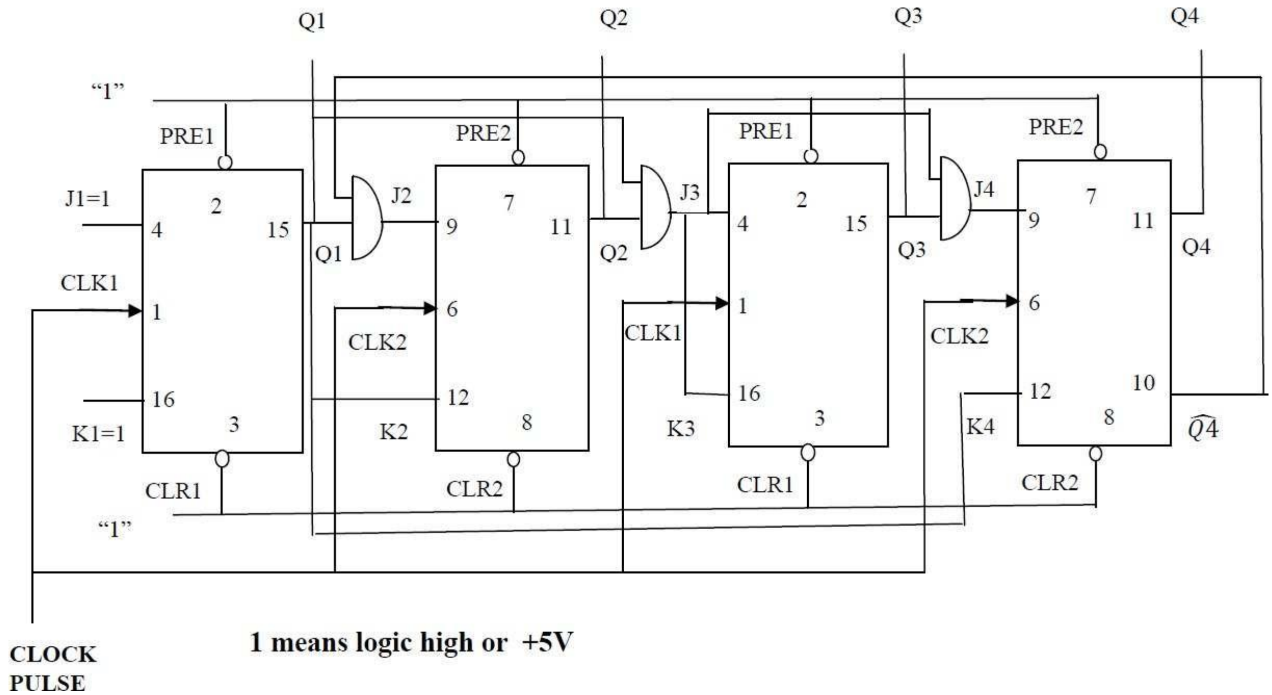
Present State				**Next State**				**Excitation Required**							
Q_4	Q_3	Q_2	Q_1	Q_4	Q_3	Q_2	Q_1	J_4	K_4	J_3	K_3	J_2	K_2	J_1	K_1

0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	0	0	0	0	X	1	0	X	0	X	X	1

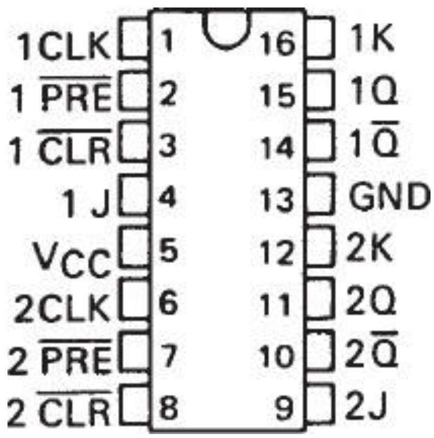
Synchronous BCD Counter Design



CIRCUIT DIAGRAM: Synchronous BCD counter using IC7476 (JK Flip Flop)



JK Flip Flop IC7476 PIN DIAGRAM



PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. Apply the input and verify the truth table of the counter

DISCUSSION QUESTIONS:

1. Compare synchronous and asynchronous sequential circuits?
2. What is a ripple counter?
3. What is propagation delay in ripple counter?
4. Define MOD counter?
5. What are the applications of counters?

6. State the types of counter?
7. Define bit, byte and word.
8. Define address of a memory.
9. What is a parallel counter?
10. What is the speed of a synchronous counter?

Result:

Thus the synchronous and asynchronous counter circuits were designed and the outputs were verified.

Ex. No: **TIMER IC APPLICATIONS - I**

Date:

STUDY OF ASTABLE MULTIVIBRATOR

AIM:

To design an astable multivibrator circuit for the given specifications using 555 Timer IC.

APPARATUS REQUIRED:

S. No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Timer IC	IC 555	1

5.	Bread Board		1
6.	Resistors	7.5KΩ, 3.9 KΩ	Each 1
7.	Capacitors	0.01µF	2
8.	Connecting wires and probes	As required	

THEORY:

An astable multivibrator, often called a free-running multivibrator, is a rectangular-wave-generating circuit. This circuit do not require an external trigger to change the state of the output. The time during which the output is either high or low is determined by two resistors and a capacitor, which are connected externally to the 555 timer. The time during which the capacitor charges from 1/3 V_{cc} to 2/3 V_{cc} is equal to the time the output is high and is given by,

$t_c = 0.69 (R_1 + R_2) C$

Similarly the time during which the capacitor discharges fro m 2/3 V_{cc} to 1/3 V_{cc} is equal to the time the output is low and is given by,

$t_d = 0.69 (R_2) C$

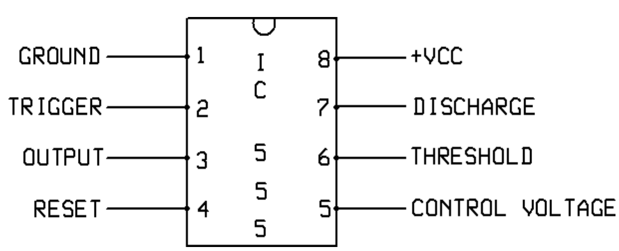
Thus the total time period of the output waveform is,

$$T = t_c + t_d = 0.69 (R_1 + 2 R_2) C$$

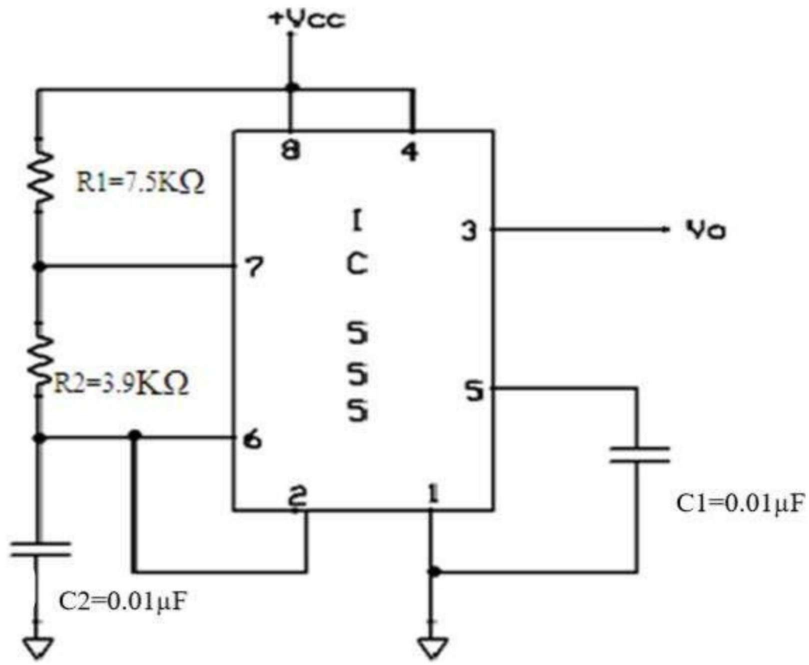
The term duty cycle is often used in conjunction with the astable multivibrator. The duty cycle is the ratio of the time t_c during which the output is high to the total time period T. It is generally expressed in percentage. In equation form,

$$\% \text{ duty cycle} = [R_2 / (R_1 + 2 R_2)] \times 100\% \text{ or } t_d / t_c \times 100\%$$

PIN DIAGRAM:



CIRCUIT DIAGRAM OF ASTABLE MULTIVIBRATOR:



DESIGN:

Given f= 11.11 KHz and duty cycle = 23%
Therefore, Total time period, $T = 1/f = 90 \times 10^{-6}$ s

We know, duty cycle = t_d / T

$23 / 100 = t_d / 90 \times 10^{-6}$, $t_d = 0.23 \times 90 \times 10^{-6}$

Therefore, $t_d = 20.7 \times 10^{-6}$ s and $t_c = T - t_d = 90 \times 10^{-6}$
$- 20.7 \times 10^{-6} = 69.3 \times 10^{-6}$ s

We also know for an astable multivibrator t_d
$= 0.69 (R_2) C$

Assume $C = 0.01 \times 10^{-6}$ F,
$R_2 = t_d /(0.69 \times C) = 20.7 \times 10^{-6} / (0.69 \times 0.01 \times 10^{-6})$

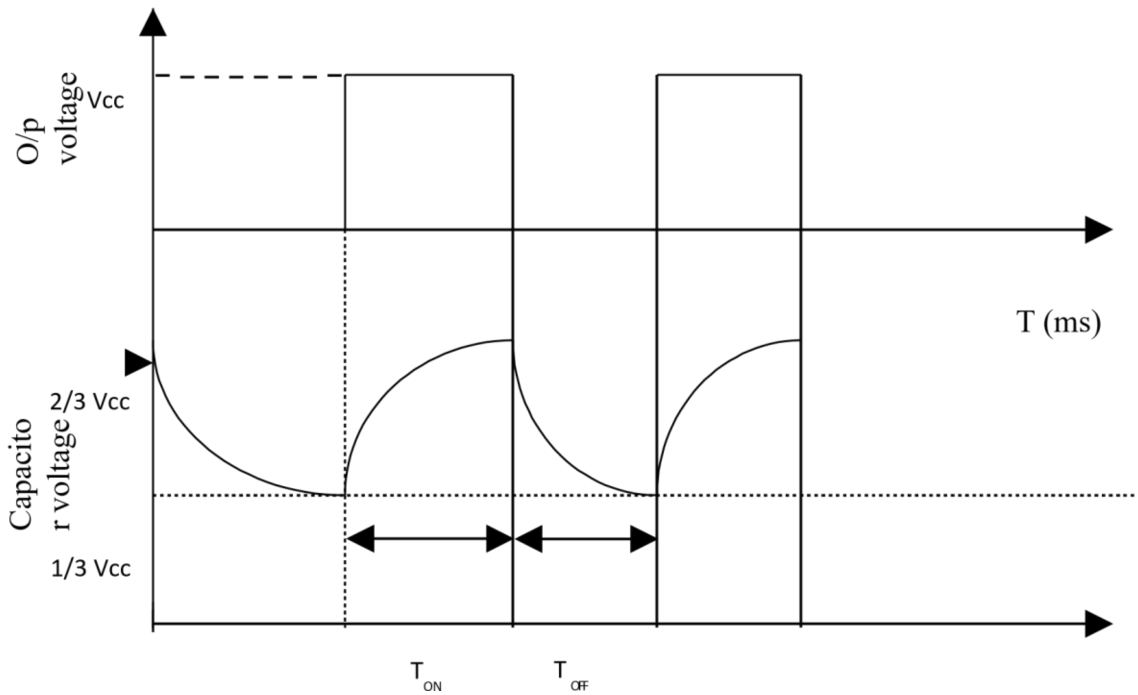
Therefore, $R_2 = 3K\Omega$ $t_c = 0.69 (R_1 + R_2) C$

$R_1 = (t_c / (0.69 \times C)) - R_2$

$R_1 = (69.3 \times 10^{-6} / (0.69 \times 0.01 \times 10^{-6})) - 3000$ Therefore,

$R_1 = 7\ K\Omega \approx 6.8\ K\Omega \approx 7.5\ K\Omega$

MODEL GRAPH:



PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + 5V supply is given to the + V_{cc} terminal of the timer IC.
3. At pin 3 the output waveform is observed with the help of a CRO
4. At pin 6 the capacitor voltage is obtained in the CRO and the V_0 and V_c voltage waveforms are plotted in a graph sheet.

OBSERVATIONS:

S.No	Waveforms	Amplitude (No. of div x Volts per div)	Time period (No. of div x Time per div)	
			t_c	t_d
1.	Output Voltage , V_o			
2.	Capacitor voltage , V_c			

DISCUSSION QUESTIONS:

1. Define Offset voltage.
2. Define duty cycle.
3. Mention the applications of IC555.
4. Give the methods for obtaining symmetrical square wave.
5. What is the other name for monostable multivibrator?
6. Explain the operation of IC555 in astable mode.. 7. Why negative pulse is used as trigger?

RESULT:

The design of the Astable multivibrator circuit was done and the output voltage and capacitor voltage waveforms were obtained.

Ex. No:

Date:

TIMER IC APPLICATIONS –II
STUDY OF MONOSTABLE MULTIVIBRATOR

AIM:

To design a monostable multivibrator for the given specifications using 555 Timer IC.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz, Analog	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Timer IC	IC 555	1
5.	Bread Board		1
6.	Resistors	10KΩ	1
7.	Capacitors	0.01µF, 0.1µF	Each 1
8.	Connecting wires and probes	As required	

THEORY:

A monostable multivibrator often called a one-shot multivibrator is a pulse generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer. In a stable or stand-by state the output of the circuit is approximately zero or at logic low level. When an external trigger pulse is applied, the output is forced to go high (approx. V_{cc}). The time during which the output remains high is given by,

$t_p = 1.1\ R_1 C$

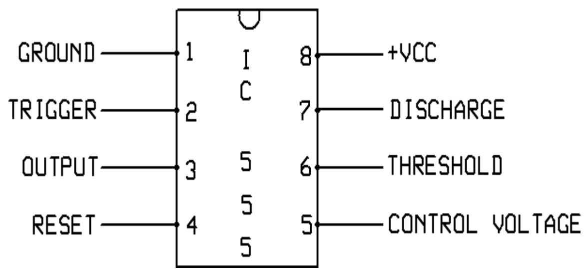
At the end of the timing interval, the output automatically reverts back to its logic low state. The output stays low until a trigger pulse is applied again. Then the cycle repeats. Thus the monostable state has only one stable state hence the name monostable.

PROCEDURE:

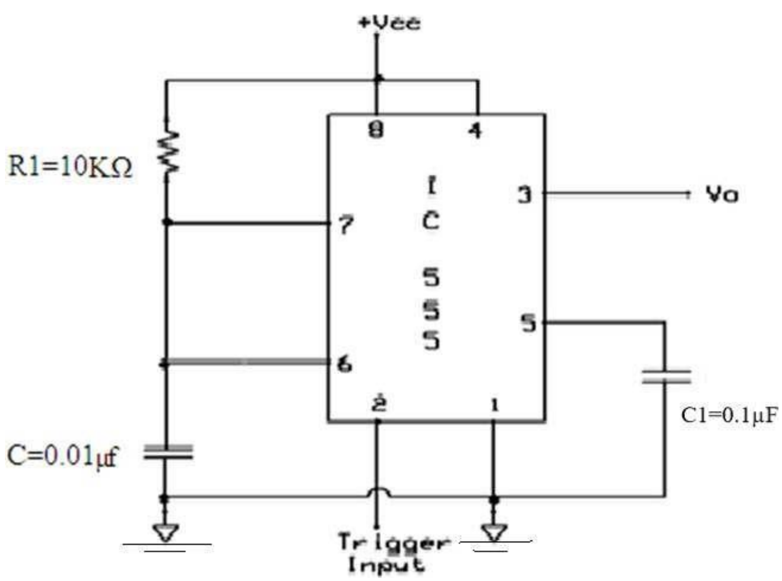
1. Connections are given as per the circuit diagram.
2. + 5V supply is given to the + V_{cc} terminal of the timer IC.
3. A negative trigger pulse of 5V, 2 KHz is applied to pin 2 of the 555 IC
4. At pin 3 the output waveform is observed with the help of a CRO

5. At pin 6 the capacitor voltage is obtained in the CRO and the V_0 and V_c voltage waveforms are plotted in a graph sheet.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF MONOSTABLE MULTIVIBRATOR:



DESIGN:

Given t_p = 0.1ms, $t_p = 1.1\ R_1\ C$

Assume C = 0.01 x 10^{-6} F,

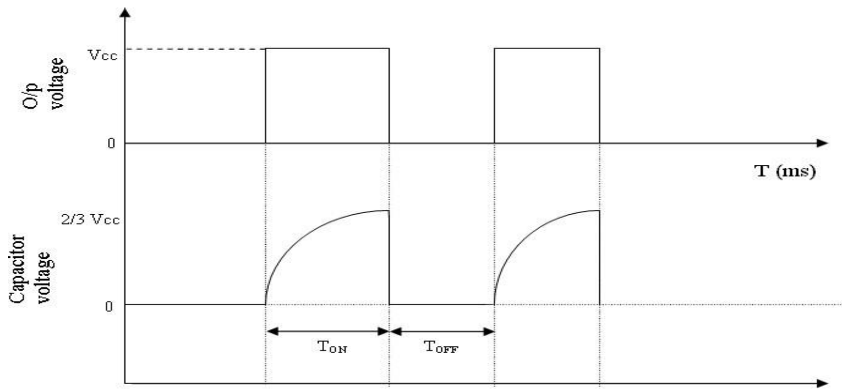
Therefore, R_1 = 9.09 KΩ ≈ 9.1 KΩ ≈ 10 KΩ

OBSERVATIONS:

S.No		Amplitude (No. of div x Volts per div)	Time period (No. of div x Time per div)	
			t_{on}	t_{off}
1.	Trigger input			
2.	Output Voltage , V_o			

3.	Capacitor voltage , V_c			

MODEL GRAPH:



DISCUSSION QUESTIONS:

1. Explain the operation of IC555 in monostable mode.
2. What is the charging time for capacitor in monostable mode?
3. What are the modes of operation of 555 timers?
4. Give the comparison between combinational circuits and sequential circuits.
5. What do you mean by present state? 6. Give the applications of 555 timers IC.

RESULT:

The design of the Monostable multivibrator circuit was done and the input and output waveforms were obtained.

Ex. No:

Date:

APPLICATIONS OF OP-AMP – I (INVERTING AND NON – INVERTING AMPLIFIER)

a. INVERTING AMPLIFIER

AIM:

To design an Inverting Amplifier for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board	1KΩ, 15KΩ	Each 1
6.	Resistors	As required	
7.	Connecting wires and probes	As required	

THEORY:

The input signal V_i is applied to the inverting input terminal through R_1 and the non- inverting input terminal of the op-amp is grounded. The output voltage V_o is fed back to the inverting input terminal through the R_f - R_1 network, where R_f is the feedback resistor. The output voltage is given as,

$$V_o = - A_{CL} V_i$$

Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal.

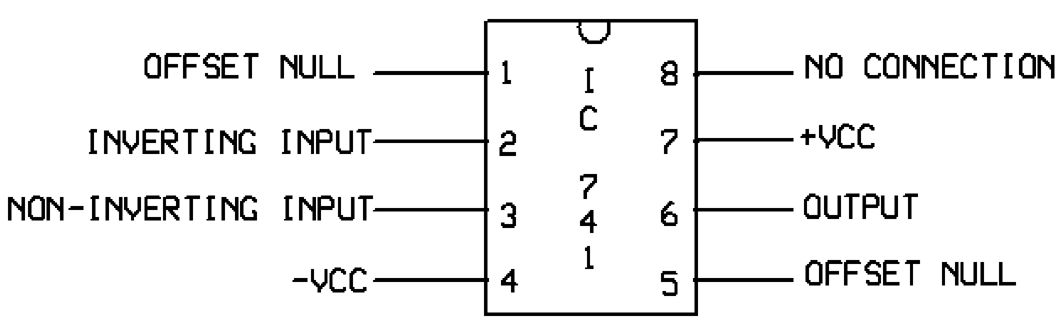
PRECAUTIONS:

1. Output voltage will be saturated if it exceeds ± 15V.

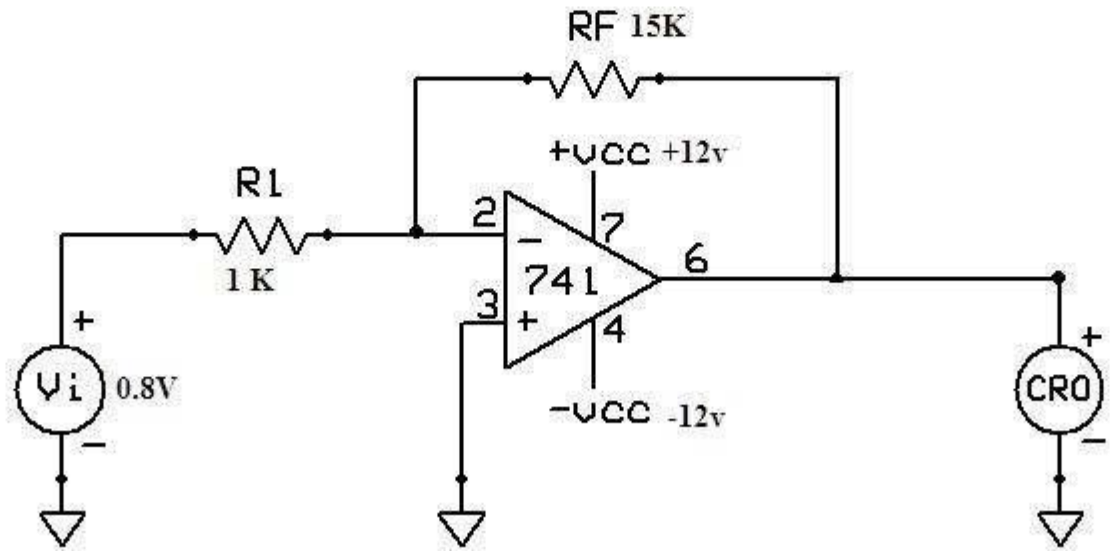
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + V_{cc} and - V_{cc} supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF INVERTING AMPLIFIER:



DESIGN:

We know for an inverting Amplifier $A_{CL} = R_F / R_1$

Assume R_1 (approx. 10 KΩ) and find R_f Hence

V_O (theoretical) $= - A_{CL} V_I$

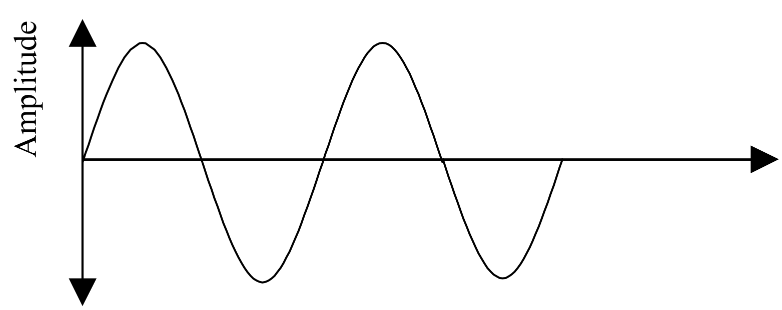
OBSERVATIONS:

S.No.	Amplitude (No. of div x Volts per div)	Time period (No. of div x Time per div)
Input		
Output	Theoretical -	
	Practical -	

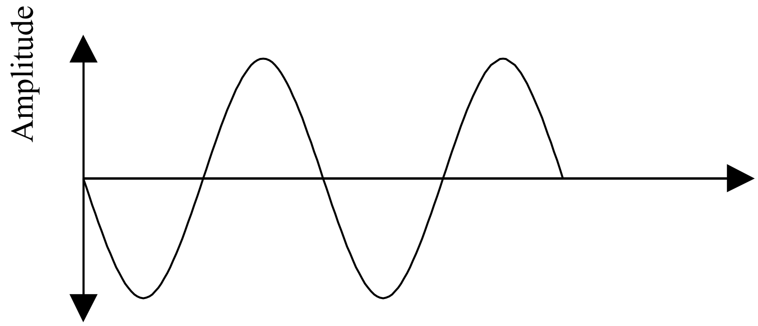
MODEL GRAPH:

<u>INVERTINGAMPLIFIER</u>:

INPUT SIGNAL:



OUTPUT SIGNAL:



RESULT:

The design and testing of the inverting amplifier is done and the input and output waveforms were drawn.

b. NON - INVERTING AMPLIFIER

AIM:

To design a Non-Inverting Amplifier for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors	1KΩ, 15KΩ	Each 1
7.	Connecting wires and probes	As required	

THEORY:

The input signal V_i is applied to the non - inverting input terminal of the op-amp. This circuit amplifies the signal without inverting the input signal. It is also called negative feedback system since the output is feedback to the inverting input terminals. The differential voltage V_d at the inverting input terminal of the op-amp is zero ideally and the output voltage is given as,

$$V_o = A_{CL} V_i$$

Here the output voltage is in phase with the input signal.

PRECAUTIONS:

1. Output voltage will be saturated if it exceeds ± 15V.

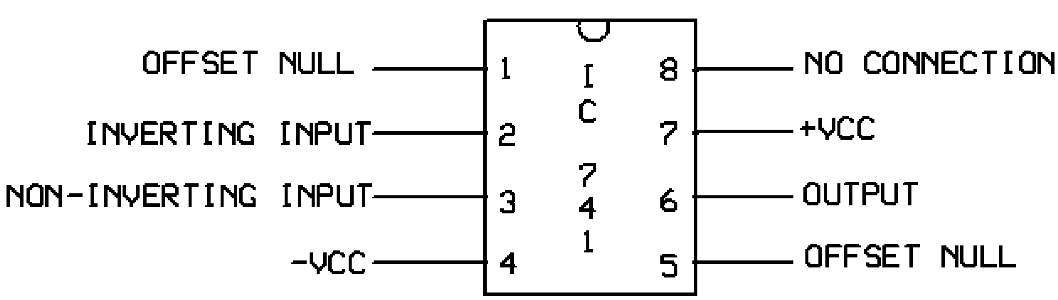
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + V_{cc} and - V_{cc} supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the non - inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

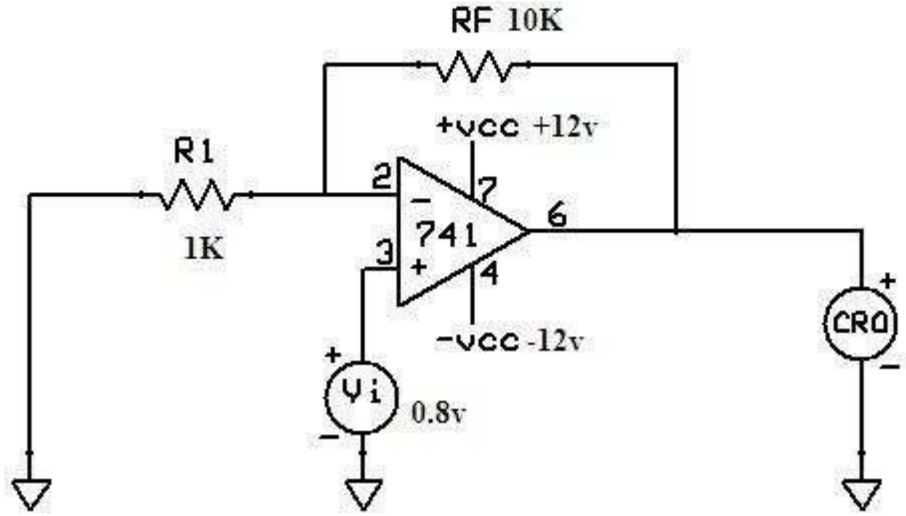
DESIGN:

We know for a Non-inverting Amplifier $A_{CL} = 1 + (R_F / R_1)$
Assume R_1 (approx. 10 KΩ) and find R_f
Hence $V_o = A_{CL} V_i$

PIN DIAGRAM:



CIRCUIT DIAGRAM OF NON INVERITNG AMPLIFIER:



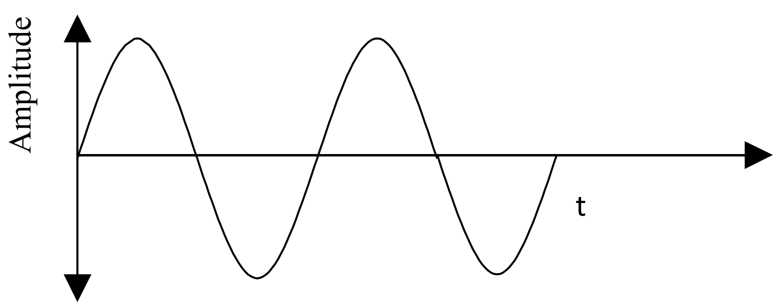
OBSERVATIONS:

S.No.	Amplitude (No. of div x Volts per div)	Time period (No. of div x Time per div)
Input		
Output	Theoretical -	
	Practical -	

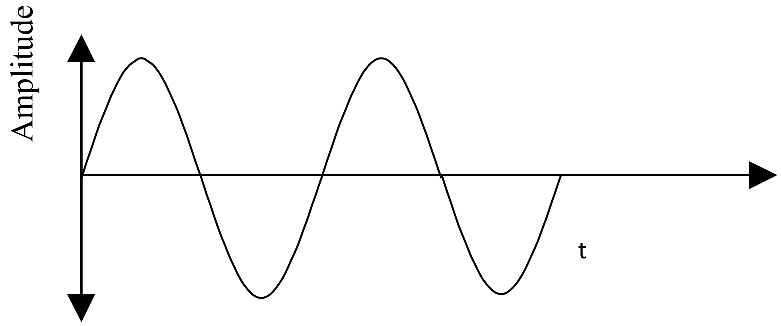
MODEL GRAPH:

NON-INVERTINGAMPLIFIER:

INPUT SIGNAL:



OUTPUT SIGNAL:



DISCUSSION QUESTIONS:

1. What do you mean by linear circuits?
2. Define an IC?
3. What is an inverting amplifier?
4. What is the type of feedback employed in the inverting op-amp
5. What is a voltage follower?
6. Define a non-inverting amplifier?
7. Give the closed loop gain of an inverting amplifier?
8. What is the gain of a non-inverting amplifier?

RESULT:

The design and testing of the Non-inverting amplifier is done and the input and output waveforms were drawn

Ex. No:

Date: **APPLICATIONS OF OP-AMP – II**

(DIFFERENTIATOR AND INTEGRATOR)

. a. DIFFERENTIATOR

AIM:

To design a Differentiator circuit for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1

6.	Resistor	1.5KΩ	1
7.	Resistor	15KΩ	2
8.	Capacitors	0.001µF, 0.01µF	Each 1
9.	Connecting wires and probes	As required	

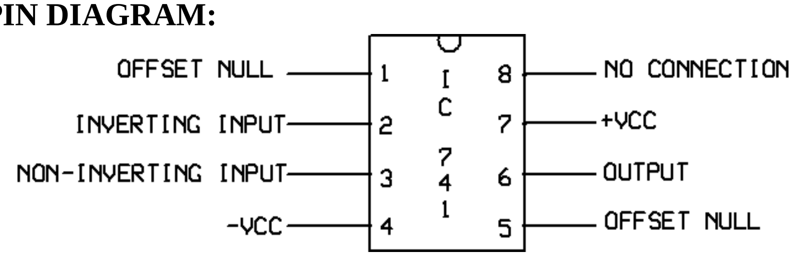
THEORY:

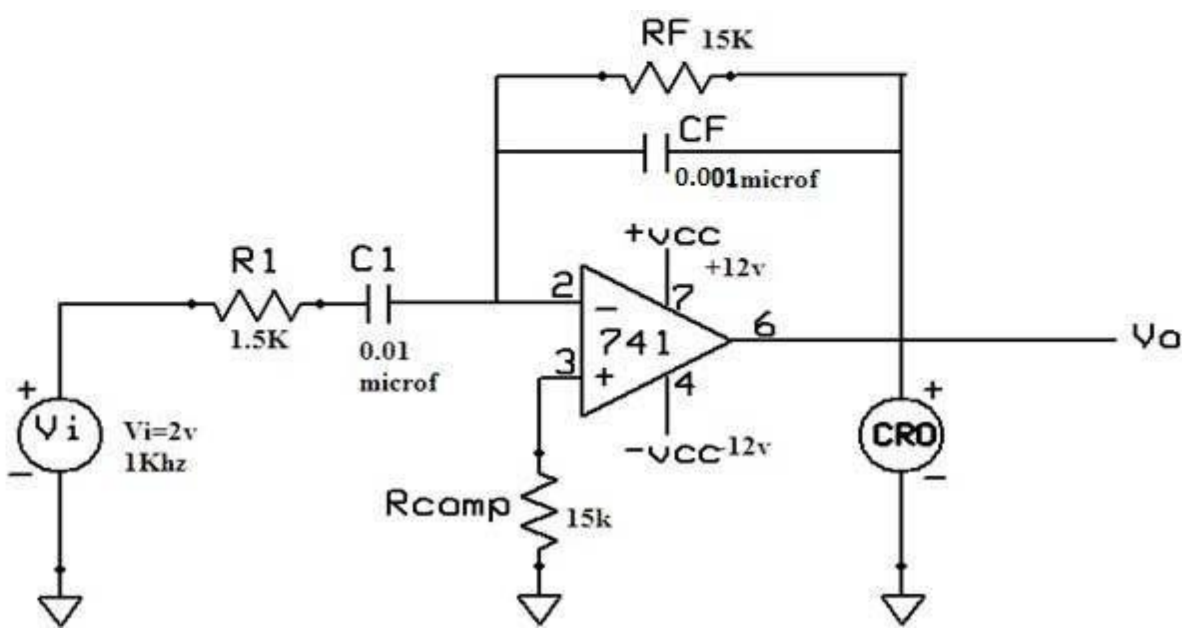
The differentiator circuit performs the mathematical operation of differentiation; that is, the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor R_1 is replaced by a capacitor C_1.
The expression for the output voltage is given as, $V_o = - R_f C_1 (dV_i /dt)$

Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal. A resistor $R_{comp} = R_f$ is normally connected to the non-inverting input terminal of the op-amp to compensate for the input bias current. A workable differentiator can be designed by implementing the following steps:

1. Select f_a equal to the highest frequency of the input signal to be differentiated. Then, assuming a value of $C_1 < 1$ µF, calculate the value of R_f.
2. Choose $f_b = 10 f_a$ and calculate the values of R_1 and C_f so that $R_1C_1 = R_f C_f$.
3. The differentiator is most commonly used in waveshaping circuits to detect high frequency components in an input signal and also as a rate–of–change detector in FM modulators.

PIN DIAGRAM:





CIRCUIT DIAGRAM OF DIFFERENTIATOR:

DESIGN:

Given $f_a = 1KHz$

We know the frequency at which the gain is 0 dB, $f_a = 1 / (2\pi R_f C_1)$

Let us assume $C_1 = 0.01 \mu F$; then

$R_f = 1/(2\pi(1 \times 10^3)(0.01 \times 10^{-6})) = 15.9K\Omega \approx 15K\Omega$

Since $f_b = 10 f_a$, $f_b = 10 KHz$

We know that the gain limiting frequency $f_b = 1 / (2\pi R_1 C_1)$

Hence $R_1 = 1 /(2\pi(10 \times 10^3)(0.01 \times 10^{-6})) = 1.59 K\Omega \approx 1.5K\Omega$

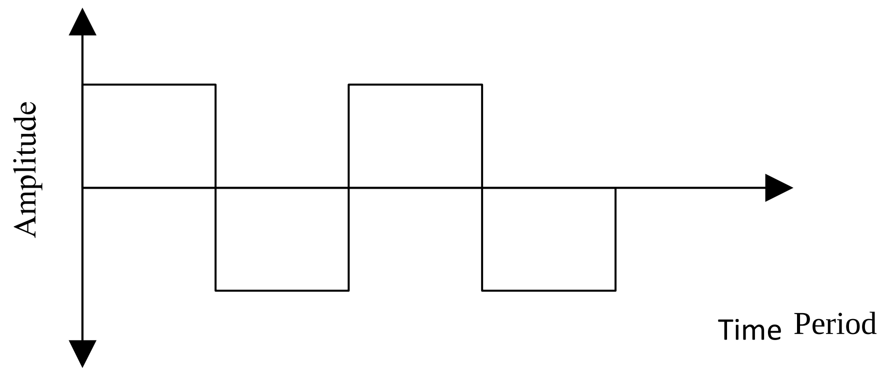
Also since $R_1C_1 = R_f C_f$; $C_f = R_1C_1 / R_f$

$C_f = (1.5 \times 10^3 \times 0.01 \times 10^{-6}) / (15 \times 10^3) = 0.001 \mu F$

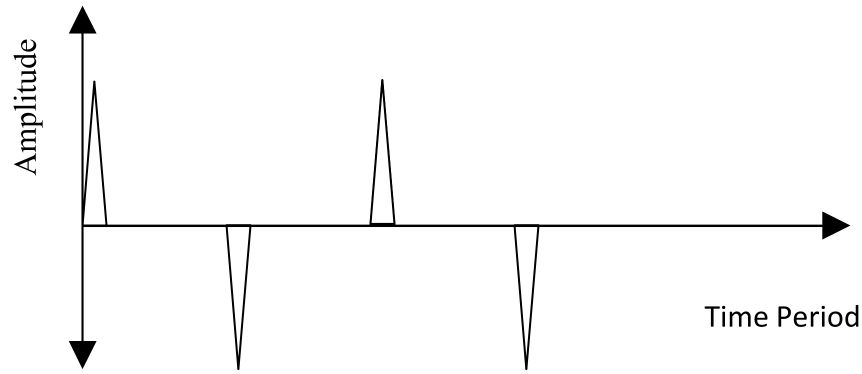
MODEL GRAPH:

<u>DIFFERENTIATOR:</u>

INPUT SIGNAL:



OUTPUT SIGNAL:



PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + V_{cc} and - V_{cc} supply is given to the power supply terminal of the Op-Amp IC.

3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

OBSERVATIONS:

Input - Sine wave

S.No.	Amplitude (No. of div x Volts per div)	Time period (No. of div x Time per div)
Input		
Output		

Input – Square wave

S.No.	Amplitude (No. of div x Volts per div)	Time period (No. of div x Time per div)
Input		
Output		

RESULT:

The design of the Differentiator circuit was done and the input and output waveforms were obtained.

b. INTEGRATOR **AIM:**

To design an Integrator circuit for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors	1.5KΩ	1
7.	Resistors	15KΩ	2
8.	Capacitors	0.01µF	1
9.	Connecting wires and probes	As required	

THEORY:

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_f is replaced by a capacitor C_f. The expression for the output voltage is given as,

$$V_o = - (1/R_f C_1) \int V_i \, dt$$

Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal. Normally between f_a and f_b the circuit acts as an integrator. Generally, the value of $f_a > f_b$. The input signal will be integrated properly if the Time period T of the signal is larger than or equal to $R_f C_f$. That is,

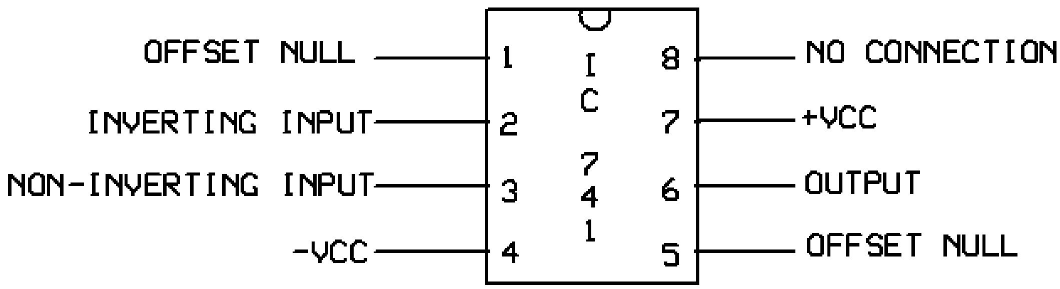
$$T \geq R_f C_f$$

The integrator is most commonly used in analog computers and ADC and signal-wave shaping circuits.

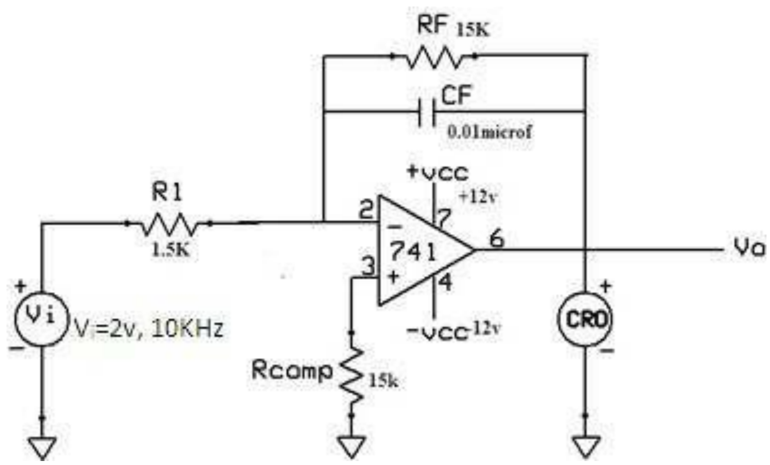
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + V_{cc} and - V_{cc} supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF INTEGRATOR:



DESIGN:

Given f_a = 10KHz

We know the frequency at which the gain is 0 dB, f_a
= 1 / (2π $R_1 C_f$)
Therefore f_b = 10KHz Since f_b = 0.1 f_a, and also the gain limiting frequency f_b = 1 / (2π R_f C_f), assume C_f = 0.01µF

R_f = 1 /(2π (1000)(0.01 x 10^{-6}) =15.9 KΩ ≈ 15KΩ

R_1=1/(2 π (10000) (0.01 x 10^{-6}) =1.59 KΩ ≈ 1.5KΩ

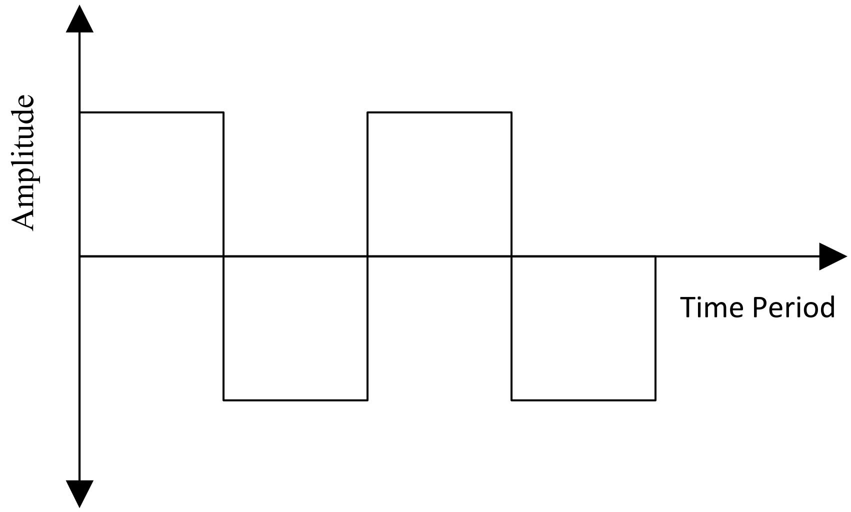
OBSERVATIONS:

S.No.	Amplitude (No. of div x Volts per div)	Time period (No. of div x Time per div)
Input		
Output		

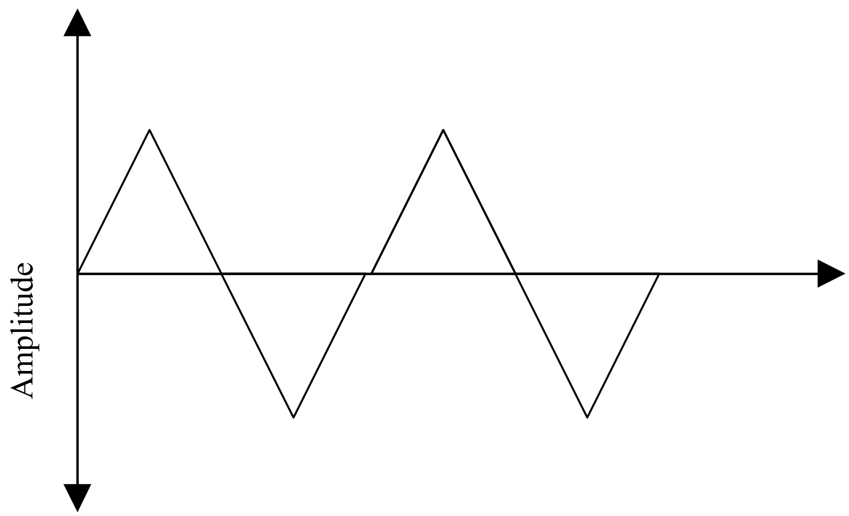
MODEL GRAPH:

INTEGRATOR:

INPUT SIGNAL:



OUTPUT SIGNAL:



DISCUSSION QUESTIONS:

1. What is integrator?
2. Write the disadvantages of ideal integrator?
3. Write the application of integrator?
4. Why compensation resistance is needed in integrator and how will you find it values?
5. What is differentiator?
6. Write the disadvantages of ideal differentiator.
7. Write the application of differentiator?
8. Why compensation resistance is needed in differentiator and how will you find it values?

9. Why integrators are preferred over differentiators in analog comparators?

RESULT:

The design of the Integrator circuit was done and the input and output waveforms were obtained.

EX-NO: Voltage to frequency characteristics of NE/ SE 566 IC.

DATE :

AIM : To study the Voltage to frequency characteristics of NE/ SE 566 IC.

Theory:

Voltage Controlled Oscillator (VCO)

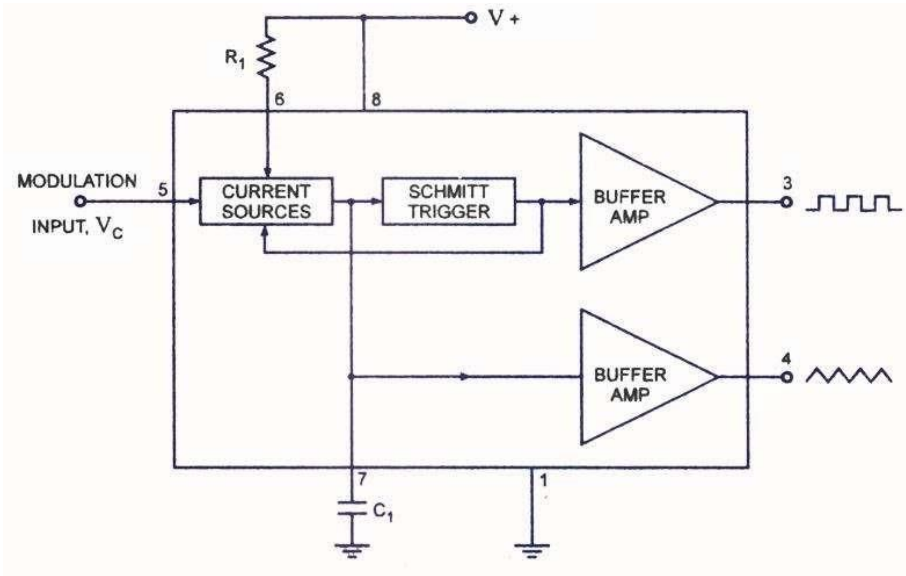
Voltage-controlled oscillator generates frequency controlled by input voltage. The dc level output of a low-pass filter is applied as control signal to the voltage-controlled oscillator (VCO). The output frequency of the VCO is directly proportional to the input dc level. The VCO frequency is adjusted till it becomes equal to the frequency of the input signal. During this adjustment, PLL goes through three stages-free running, capture and phase lock. Best operation is obtained if the centre frequency of the VCO is set with the dc bias voltage midway in its linear operating range. The amplifier allows this adjustment in dc voltage from that obtained as output of the filter circuit. When the loop is in lock, the two signals to the PC are necessarily of the same frequency although not necessarily in phase. A fixed phase difference between the two signals to the comparator results in a fixed dc voltage to the VCO. Variation in the input signal frequency then causes variation in the dc voltage to the VCO. Within a capture-and-Iock frequency range, the dc voltage will drive the VCO frequency to match that of the input.

While the loop is trying to achieve lock, the output of the PC contains frequency components at the sum and difference of the signals compared. A low-pass filter passes only the lower-frequency component of the signal so that the loop can obtain lock between input and VCO signals.

Owing to the limited operating range of the VCO and the feedback connection of the PLL circuit, there are two important frequency bands specified for a PLL. The capture range of a PLL is the range of frequencies centred about the VCO free-running frequency f_r, over which the output signal frequency of the VCO can acquire lock with the input signal frequency. Once the PLL has achieved capture, it can maintain lock with the input signal over a somewhat wider frequency range called the lock range.

In most cases, the frequency of an oscillator is determined by the time constant RC. However, in cases or applications such as FM, tone generators, and frequency-shift keying (FSK), the frequency is to be controlled by means of an input voltage, called the control voltage. This can be achieved in a voltage-controlled oscillator (VCO). *A VCO is a circuit that provides an oscillating output signal (typically of square-wave or triangular waveform) whose frequency can be adjusted over a range by a dc voltage.* An example of a *VCO is th*e 566 IC unit, that provides simultaneously the square-wave and triangular-wave outputs as a function of input voltage. The frequency of oscillation is set by an external resistor R_1 and a capacitor C_1 and the voltage V_c applied to the control terminals.

Voltage controlled oscillator

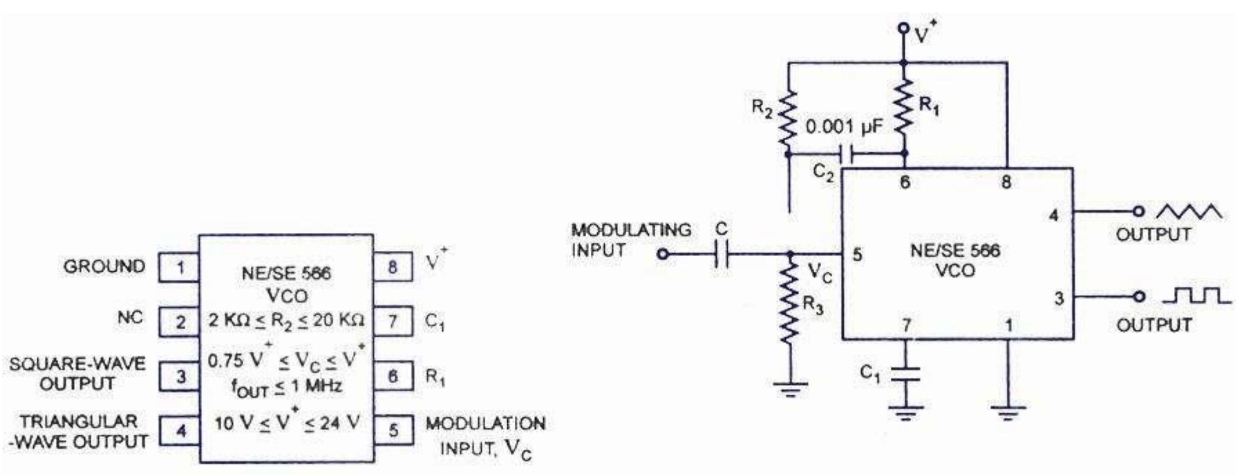


(a) Block Diagram

Figure shows that the 566 IC unit contains current sources to charge and discharge an external capacitor C_v at a rate set by an external resistor R_1 and the modulating dc input voltage. A Schmitt trigger circuit is employed to switch the current sources between charging and discharging the capacitor, and the triangular voltage produced across the capacitor and square-wave from the Schmitt trigger are provided as outputs through buffer amplifiers. Both the output waveforms are buffered so that the output impedance of each is 50 f2. The typical magnitude of the triangular wave and the square wave are 2.4 $\mathbf{V_{peak\text{-}to\text{-}peak}}$ **and** $\mathbf{5.4V_{peak\text{-}to\text{-}peak}}$.

The frequency of the output waveforms is approximated by

$$\mathbf{f_{out} = 2(V^+ - V_c)/R_1C_1V^+}$$



(b) Pin Configuration

(c) Typical Connection Diagram

Voltage Controlled Oscillator

The VCO can be programmed over a 10-to-l frequency range by proper selection of an external resistor and capacitor, and then modulated over a 10-to-l frequency range by a control voltage, V_c The voltage controlled oscillators (VCOs) are commonly used in converting low-frequency signals such as EEG (electro-encephalograms) or ECG (electro-cardiograms) into an audiofrequency (AF range)

Result:

CONTENT BEYOND SYLLABUS

Ex. No: **STUDY OF FLIP FLOPS**

Date:

AIM:

To verify the characteristic table of RS, D, JK, and T Flip flops .

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	NOR gate	IC 7402	
3.	NOT gate	IC 7404	
4.	AND gate (three input)	IC 7411	
5.	NAND gate	IC 7400	
6.	Connecting wires		As required

THEORY:

A Flip Flop is a sequential device that samples its input signals and changes its output states only at times determined by clocking signal. Flip Flops may vary in the number of inputs they possess and the manner in which the inputs affect the binary states.

RS FLIP FLOP:

The clocked RS flip flop consists of NAND gates and the output changes its state with respect to the input on application of clock pulse. When the clock pulse is high the S and R inputs reach the second level NAND gates in their complementary form. The Flip Flop is reset when the R input high and S input is low. The Flip Flop is set when the S input is high and R input is low. When both the inputs are high the output is in an indeterminate state.

D FLIP FLOP:

To eliminate the undesirable condition of indeterminate state in the SR Flip Flop when both inputs are high at the same time, in the D Flip Flop the inputs are never made equal at the same time. This is obtained by making the two inputs complement of each other.

JK FLIP FLOP:

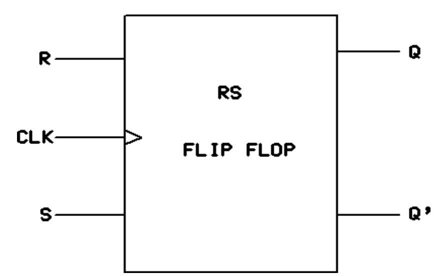
The indeterminate state in the SR Flip-Flop is defined in the JK Flip Flop. JK inputs behave like S and R inputs to set and reset the Flip Flop. The output Q is ANDed with K input and the clock pulse, similarly the output Q' is ANDed with J input and the Clock pulse. When the clock pulse is zero both the AND gates are disabled and the Q and Q' output retain their previous values. When the clock pulse is high, the J and K inputs reach the NOR gates. When both the inputs are high the output toggles continuously.

This is called Race around condition and this must be avoided. T
FLIP FLOP:

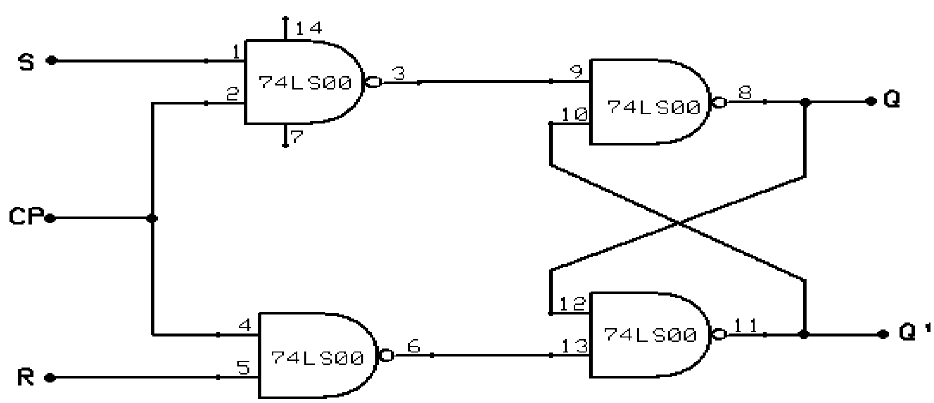
This is a modification of JK Flip Flop, obtained by connecting both inputs J and K inputs together. T Flip Flop is also called Toggle Flip Flop.

RS FLIP FLOP

LOGIC SYMBOL:



CIRCUIT DIAGRAM:

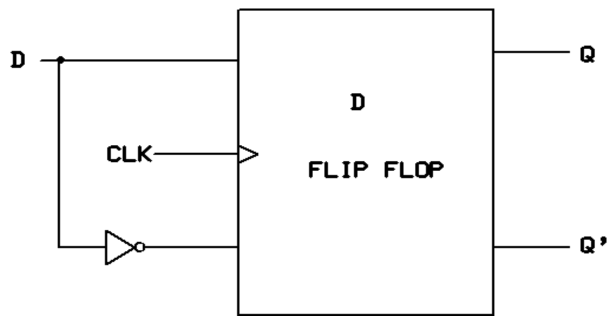


CHARACTERISTIC TABLE:

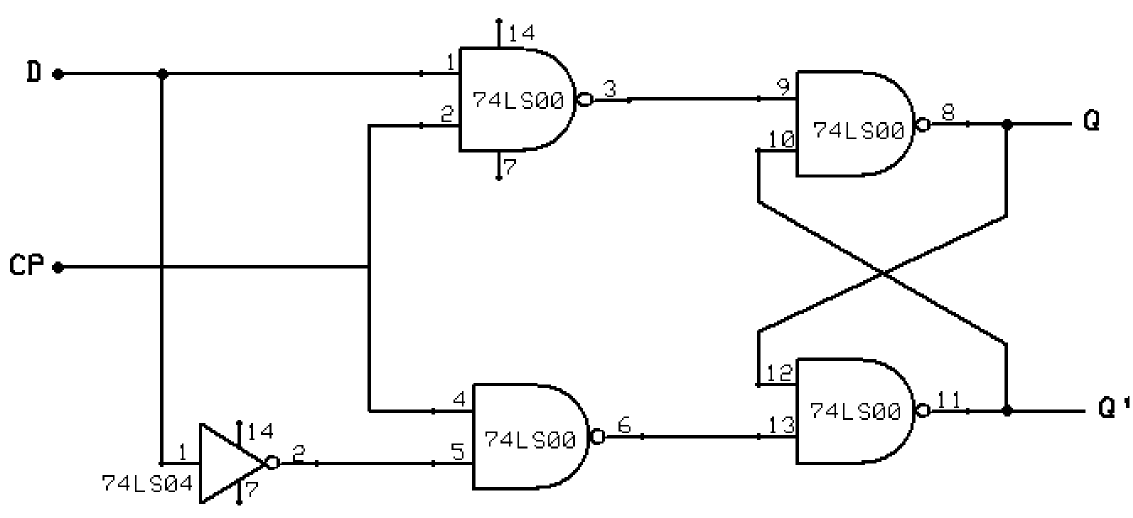
CLOCK PULSE	IN PUT		PRESENT STATE (Q)	NEXT STATE(Q+1)	STATUS
	S	R			
1	0	0	0	0	
2	0	0	1	1	
3	0	1	0	0	
4	0	1	1	0	
5	1	0	0	1	
6	1	0	1	1	
7	1	1	0	X	
8	1	1	1	X	

D FLIP FLOP

LOGIC SYMBOL:



CIRCUIT DIAGRAM:



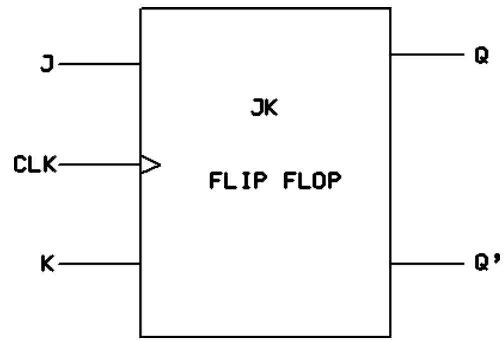
CHARACTERISTIC TABLE:

CLOCK PULSE	INPUT D	PRESENT STATE (Q)	NEXT STATE(Q+1)	STATUS
1	0	0	0	
2	0	1	0	

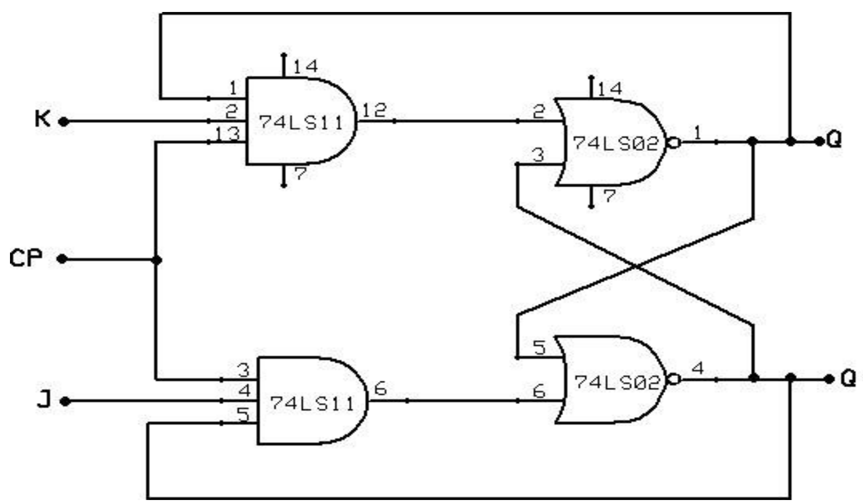
3	1	0	1	
4	1	1	1	

JK FLIP FLOP

LOGIC SYMBOL:



CIRCUIT DIAGRAM:



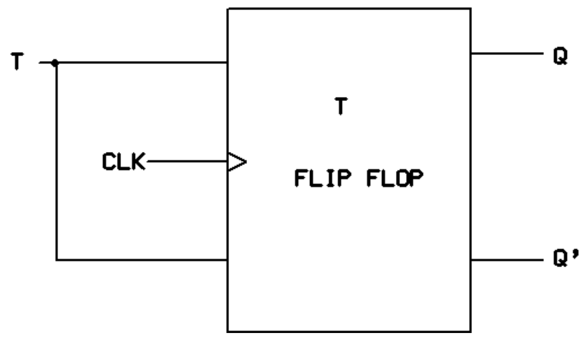
CHARACTERISTIC TABLE:

CLOCK PULSE	IN PUT		PRESENT STATE (Q)	NEXT STATE(Q+1)	STATUS
	J	K			
1	0	0	0	0	
2	0	0	1	1	
3	0	1	0	0	
4	0	1	1	0	
5	1	0	0	1	
6	1	0	1	1	

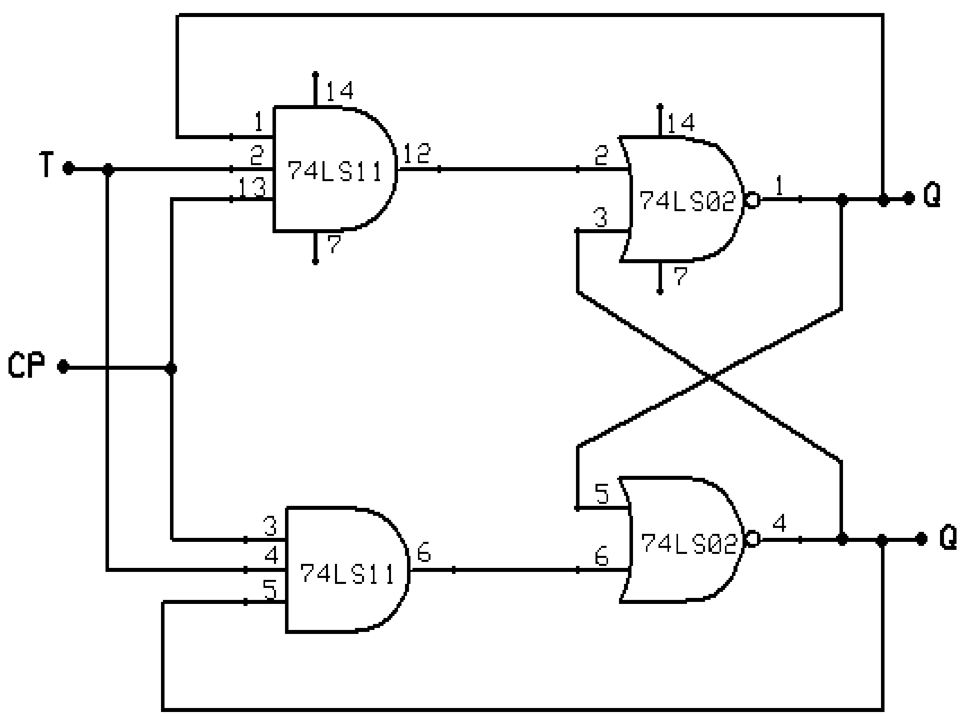
7	1	1	0	1	
8	1	1	1	0	

T FLIPFLOP

LOGIC SYMBOL:



CIRCUIT DIAGRAM:



CHARACTERISTIC TABLE:

CLOCK PULSE	INPUT T	PRESENT STATE (Q)	NEXT STATE(Q+1)	STATUS
1	0	0	0	
2	0	1	0	
3	1	0	1	

4	1	1	0	

PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. For all the ICs 7th pin is grounded and 14th pin is given +5 V supply. 3. Apply the inputs and observe the status of all the flip flops.

DISCUSSION QUESTIONS:

1. Define flip-flop
2. What is race around condition?
3. Explain the flip-flop excitation tables for D flip-flop 4. Explain the flip-flop excitation tables for JK flip-flop
5. What is a master-slave flip-flop?
6. What is edge-triggered flip-flop?
7. What is the operation of D flip-flop?
8. What are the different types of flip-flop?

RESULT:

The Characteristic tables of RS, D, JK, T flip flops were verified