AL-AMEEN ENGINEERING COLLEGE

(Autonomous)

(Accredited by NAAC with "A" Grade :: An ISO Certified Institution)
(Affiliated to Anna University, Chennai & Approved by AICTE, New Delhi)
Karundevanpalayam, Nanjai Uthukkuli Post, Erode – 638 104, Tamilnadu, INDIA.

CURRICULUM & SYLLABI

SEMESTERS – I to IV

(Regulations 2020)

CHOICE BASED CREDIT SYSTEM

M.E. VLSI DESIGN

Applicable to the Students from the AY 2021-22 onwards

VISION	
	To develop quality, innovative and confident engineers in the field of Electronics and Communication with research focus and social responsibilities those who can adhere and face the global challenges.

MISSION	
	To create a unique learning environment equipped to face different challenges in industry and research areas in the related field.
	To develop soft skills and solve the complex technological problems of the modern society.
	To create competent professionals by imparting wide analysed methodology and to develop the spirit of innovative communication by establishing the centre of excellence.

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)	
PEO 1	Attain mastery in applying VLSI concepts to Engineering problems so as to meet the need of the industry, teaching, higher education or research.
PEO 2	Creation of expertise in the microelectronics domain to deal with design, development, analysis, testing and evaluation of the critical aspects of integrated circuits and its core concepts.
PEO 3	To exhibit professional competence and leadership qualities with harmonious blend of ethics leading to an integrated personality development.

PROGRAM OUTCOMES (POs)	
PO 1	Acquire in-depth knowledge in the field of VLSI Design with an ability to evaluate and analyse the existing knowledge for enhancement
PO 2	Analyse critical complex engineering problems and provide solutions through research
PO 3	Identity the areas for the development of Electronic hardware design for the benefit of the society

PO 4	Extract information pertinent to challenging problems through literature survey and by applying appropriate research methodologies, techniques and tools to the development of technological knowledge
PO 5	Select, learn and apply appropriate techniques, resources and modern engineering tools to complex engineering activities with an understanding of limitations
PO 6	Understand group dynamics, recognise opportunities and contribute positively to multidisciplinary work to achieve common goals for further learning
PO 7	Demonstrate engineering principles and apply the same to manage projects efficiently as a team after considering economical and financial factors
PO 8	Communicate with engineering community and society regarding complex engineering activities effectively through reports, design documentation and presentations
PO 9	Engage with commitment in life-long learning independently to improve knowledge and competence
PO 10	Acquire professional and intellectual integrity, professional code and conduct, ethics of research and scholarship by considering the research outcomes to the community for sustainable development of society
PO 11	Observe and examine critically the outcomes and make corrective measures, and learn from mistakes without depending on external feedback
PO 12	Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSOs)	
PSO 1	To design and develop VLSI circuits to optimise power and area requirements, free from faults and dependencies by modelling, simulation and testing.
PSO 2	To develop VLSI systems by learning advanced algorithms, architectures and software –hardware co –design.

CURR ICULUM

SEMESTER I

Sl. No.	Course Code	Course Title	Category	CIA	ESE	L	T	P	C
THEORY									
1	20MV1T1	Applied Mathematics for Electronics Engineers	FC	40	60	3	1	0	4
2	20MV1T2	Advanced Digital System Design	PC	40	60	3	0	0	3
3	20MV1T3	CMOS VLSI Design	PC	40	60	3	0	0	3
4	20MV1T4	System Design using FPGA	PC	40	60	3	0	0	3
5	20MV1T5	Device Modeling and Simulation	PC	40	60	3	0	0	3
6	20MV1E1 to 20MV1E3	Professional Elective-I	PE	40	60	3	0	0	3
LABORATORY									
7	20MV1L1	VLSI Design Laboratory –I	PC	60	40	0	0	3	1.5
8	20MV1L2	Seminar and Technical Writing	EEC	100	--	0	0	2	1
Total						**18**	**1**	**5**	**21.5**

SEMESTER II

Sl. No.	Course Code	Course Title	Category	CIA	ESE	L	T	P	C
THEORY									
1	20MV2T1	Low power CMOS Circuits and Memories	PC	40	60	3	0	0	3
2	20MV2T2	Mixed Signal Circuit Design	PC	40	60	3	0	0	3
3	20MV2T3	Testing of VLSI Circuits	PC	40	60	3	0	0	3
4	20MV2T4	CAD for VLSI Circuits	PC	40	60	3	0	0	3
5	20MV2E1 to 20MV2E3	Professional Elective-II	PE	40	60	3	0	0	3
6	20MV2E4 to 20MV2E6	Professional Elective-III	PE	40	60	3	0	0	3
LABORATORY									
7	20MV2L1	VLSI Design Laboratory – II	PC	60	40	0	0	3	1.5
8	20MV2L2	Mini project	EEC	100	--	0	0	3	1.5
Total						**18**	**0**	**6**	**21**

SEMESTER III

Sl. No.	Course Code	Course Title	Category	CIA	ESE	L	T	P	C
THEORY									
1	20MV3E1 to 20MV3E3	Professional Elective-IV	PE	40	60	3	0	0	3
2	20MV3E4 to 20MV3E6	Professional Elective-V	PE	40	60	3	0	0	3
LABORATORY									
3	20MV3L1	Project work Phase –I	EEC	60	40	0	0	20	10
Total						6	0	20	16

SEMESTER IV

Sl. No.	Course Code	Course Title	Category	CIA	ESE	L	T	P	C
LABORATORY									
1	20MV4L1	Project work Phase –II	EEC	60	40	0	0	30	15
Total						0	0	30	15

FUNDAMENTAL COURSE (FC)

Sl.No.	Course Code	Course Title	L	T	P	C
1.	20MV1T1	Applied Mathematics for Electronics Engineers	3	1	0	4

PROFESSIONAL CORE (PC)

Sl.No.	Course Code	Course Title	L	T	P	C
1.	20MV1T2	Advanced Digital System Design	3	0	0	3
2.	20MV1T3	CMOS VLSI Design	3	0	0	3
3.	20MV1T4	System Design using FPGA	3	0	0	3
4.	20MV1T5	Device Modeling and Simulation	3	0	0	3
5.	20MV1L1	VLSI Design Laboratory –I	0	0	3	1.5
6.	20MV2T1	Low power CMOS Circuits and Memories	3	0	0	3
7.	20MV2T2	Mixed Signal Circuit Design	3	0	0	3
8.	20MV2T3	Testing of VLSI Circuits	3	0	0	3
9.	20MV2T4	CAD for VLSI Circuits	3	0	0	3
10.	20MV2L1	VLSI Design Laboratory – II	0	0	3	1.5

PROFESSIONAL ELECTIVES (PE)

Semester – I (Elective I)						
Sl.No.	**Course Code**	**Course Title**	**L**	**T**	**P**	**C**
1	20MV1E1	Advanced Computer Architecture and Parallel Processing	3	0	0	3
2	20MV1E2	Semiconductor Device Modeling	3	0	0	3
3	20MV1E3	Nano Electronics	3	0	0	3

Semester – II (Elective II)						
Sl.No.	**Course Code**	**Course Title**	**L**	**T**	**P**	**C**
1	20MV2E1	Signal Integrity for High Speed Devices	3	0	0	3
2	20MV2E2	High Speed Digital Design	3	0	0	3
3	20MV2E3	DSP Integrated Circuits	3	0	0	3

Semester – II (Elective III)						
Sl.No.	**Course Code**	**Course Title**	**L**	**T**	**P**	**C**
1	20MV2E4	ASIC Design	3	0	0	3
2	20MV2E5	Microsensors and MEMS	3	0	0	3
3	20MV2E6	Advanced Embedded System Design	3	0	0	3

Semester – III (Elective IV)						
Sl.No.	**Course Code**	**Course Title**	**L**	**T**	**P**	**C**
1	20MV3E1	Data Converters	3	0	0	3
2	20MV3E2	VLSI Technology	3	0	0	3
3	20MV3E3	VLSI for Wireless Communication	3	0	0	3

Semester – III (Elective V)						
Sl.No.	**Course Code**	**Course Title**	**L**	**T**	**P**	**C**
1	20MV3E4	Analog VLSI Circuits	3	0	0	3
2	20MV3E5	Radio Frequency IC Design	3	0	0	3
3	20MV3E6	Baseband Algorithms on FPGA	3	0	0	3

EMPLOYABILITY ENHANCEMENT COURSES (EEC)

Sl. No.	Course Code	Course Title	L	T	P	C
1.	20MV1L2	Seminar and Technical Writing	0	0	2	1
2.	20MV2L2	Mini project	0	0	3	1.5
3.	20MV3L1	Project work Phase –I	0	0	20	10
4.	20MV4L1	Project work Phase –II	0	0	32	15

CURRICULUM BREAKDOWN STRUCTURE

Subject	Total number of credits	% of Credits
Fundamental Course (FC)	**4**	**5.44**
Professional Core (PC)	**27**	**36.73**
Professional Electives (PE)	**15**	**20.41**
Employability Enhancement Courses (EEC)	**27.5**	**37.41**
Total	**73.5**	**100**

CREDIT SUMMARY

Sl. No.	Subject Area	Credits per Semester				Total Credits
		I	II	III	IV	
1	**FC**	4				4
2	**PC**	13.5	13.5			27
3	**PE**	3	6	6		15
4	**EEC**	1	1.5	10	15	27.5
TOTAL		**21.5**	**21**	**16**	**15**	**73.5**

SEMESTER I

Sl. No.	Course Code	Course Title	Category	CIA	ESE	L	T	P	C
THEORY									
1	20MV1T1	Applied Mathematics for Electronics Engineers	FC	40	60	3	1	0	4
2	20MV1T2	Advanced Digital System Design	PC	40	60	3	0	0	3
3	20MV1T3	CMOS VLSI Design	PC	40	60	3	0	0	3
4	20MV1T4	System Design using FPGA	PC	40	60	3	0	0	3
5	20MV1T5	Device Modeling and Simulation	PC	40	60	3	0	0	3
6	20MV1E1 to 20MV1E3	Professional Elective-I	PE	40	60	3	0	0	3
LABORATORY									
7	20MV1L1	VLSI Design Laboratory –I	PC	60	40	0	0	3	1.5
8	20MV1L2	Seminar and Technical Writing	EEC	100	--	0	0	2	1
Total						**18**	**1**	**5**	**21.5**

Semester	Programme	Course Code	Course Name	L	T	P	C
I	M.E. VLSI DESIGN	20MV1T1	APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS	3	1	0	4

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Interpret the concept of fuzzy logic, matrix theory, random variables, dynamic programming and queuing models for applying the interpretations in selection and use of appropriate mathematical techniques	K2	1,2,3,4,5
CO2	Concepts of fuzzy sets, knowledge representation using fuzzy rules, fuzzy logic, fuzzy prepositions and fuzzy quantifiers and applications of fuzzy logic.	K3	1
CO3	Apply various methods in matrix theory to solve system of linear equations.	K3	2
CO4	Analyze the principle of optimality and sub-optimization, formulation and computational procedure of dynamic programming.	K4	4
CO5	Relate and apply the concept of probability and random variables and predict probabilities of events in models following normal distribution.	K3	3
CO6	Choose the appropriate methods in a queue discipline to develop a relationship between the queue length and service time distribution Laplace transforms for M/G/1 queue.	K6	5

PRE-REQUISITE	NIL

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	3		1	1				1			1	1	
CO2	1	2							1				1	
CO3	1	1	1									1	1	
CO4	1	1							1				1	
CO5	1	1		1								1	1	
CO6	2	1							1				1	

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignments
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**FUZZY LOGIC**	**9 + 3**
Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers		
Topic - 2	**MATRIX THEORY**	**9 + 3**
Fuels: Introduction - classification of fuels – Combustion- coal – Analysis of coal - carbonization - manufacture of metallurgical coke (Otto Hoffmann method) - petroleum - knocking - octane number - diesel oil - cetane number - natural gas - compressed natural gas (CNG) - liquefied petroleum gases (LPG) - power alcohol.		
Topic - 3	**PROBABILITY AND RANDOM VARIABLES**	**9 + 3**
Probability – Axioms of probability – Conditional probability – Baye's theorem - Random variables - Probability function – Moments – Moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random variable.		
Topic - 4	**DYNAMIC PROGRAMMING**	**9 + 3**
Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming: Cargo loading method – Workforce size model – Equipment replacement model. – Problem of dimensionality		
Topic - 5	**QUEUEING MODELS**	**9 + 3**
Poisson Process – Markovian queues – Single and multi server models – Little‟s formula - Machine interference model – Steady state analysis – Self service queue		

THEORY	**45**		**TUTORIAL**	**15**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	Bronson, R., "Matrix Operations", Schaum's Outline Series, McGraw Hill, 2011
2	George, J. Klir. and Yuan, B., "Fuzzy sets and Fuzzy logic, Theory and Applications", Prentice Hall of India Pvt. Ltd., 2015
3	Gross, D., Shortle J. F., Thompson, J.M., and Harris, C. M., "Fundamentals of Queueing Theory", 4th Edition, John Wiley, 2014
4	Johnson, R.A., Miller, I and Freund J., "Miller and Freund‟s Probability and Statistics for Engineers", Pearson Education, Asia, 8th Edition, 2015
5	Taha, H.A., "Operations Research: An Introduction", 9th Edition, Pearson Education, Asia, New Delhi, 2016.

OTHER REFERENCES	
1	**https://www.cuemath.com/learn/mathematics/probability-in-real-life/**
2	**https://sciencing.com/examples-of-real-life-probability-12746354.html**
3	**http://www.iraj.in/journal/journal_file/journal_pdf/14-358-149822091462-64.pdf**

Semester	Programme	Course Code	Course Name	L	T	P	C
I	M.E. VLSI DESIGN	20MV1T2	ADVANCED DIGITAL SYSTEM DESIGN	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Explain and articulate the concepts of advanced digital system design	K2	1,2,3,4,5
CO2	Apply the concept of synchronous and asynchronous circuits in building digital systems	K3	1,2
CO3	Compare the synchronous and asynchronous circuits design to rate the performance	K4	1,2
CO4	Analyze the design to infer its limitations	K4	3,4,5
CO5	Evaluate the applications and recommend a suitable design	K5	3,5
CO6	Design a digital system for a given application	K6	3,5

PRE-REQUISITE	NIL

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	2	2	2		1		1				2	
CO2	2	2	1				1					1	1	
CO3	3	2	2	2	2		2					1	1	
CO4	2	1	2	2	1		2		1					2
CO5	2	2	2	1	1							1	1	
CO6	3	2	1	2	1		1		1				3	

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**SYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN**	**9**
Analysis of clocked synchronous sequential circuits - Moore / Mealy State diagrams - State table - State Reduction and Assignment - Design of synchronous sequential circuits.		
Topic - 2	**ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN**	**9**
Analysis of asynchronous sequential circuit - Cycles - Races - Static, Dynamic and Essential hazards - Primitive Flow Table - State Reductions and State Assignment - Design of asynchronous sequential circuits.		
Topic - 3	**DESIGN OF SYSTEM CONTROLLER USING COMBINATIONAL AND SEQUENTIAL CIRCUIT**	**9**
System Controllers - Design Phases - Choosing the controller architecture - State Assignment - Next State decoder - Examples of 2s complement system and Pop Vending Machine - Decoders and Multiplexers in system controllers - Indirect-Addressed MUX configuration - System controllers using ROM, Shift Registers and Counters - General requirements of a programmable controller - Microinstructions - Programmable controllers with fixed instruction set.		
Topic - 4	**INTRODUCTION TO VHDL**	**9**
VHDLDescription of Combinational circuits - VHDL Modules - Sequential Statements and VHDLProcesses- Modeling Flip-Flops - Processes Using Wait Statements - Transport and Inertial Delays - Data Types and Operators - Modeling Multiplexers, registers and Counters -Behavioral and structural VHDL - Variables, Signals, Constants - Arrays-loops.		
Topic - 5	**SM CHARTS AND FLOATING -POINT ARITHMETIC**	**9**
State Machine Chart - Derivation of SM Charts - Realization of SM Charts - Implementation of the Dice-Game - Microprogramming - Linked state machines - Representation of Floating-Point Numbers - Floating-point Multiplication - Floating-Point Addition - Other Floating-Point Operations.		

THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	**William I. Fletcher, "An Engineering Approach to Digital Design", Prentice Hall India, 2011.**
2	**Charles H.Roth Jr "Digital Systems Design using VHDL,"Cengage Learning, 2013.**
3	**Nripendra N Biswas "Logic Design Theory" Prentice Hall, 2001.**
4	**Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL", 2nd Edition, Prentice Hall, 2002.**
5	**Mark Zwolinski, "Digital System Design with VHDL, 2nd Edition, Pearson Education, 2004.**
6	**Stephen Brown,Zvonko Vranesic, "Digital system Design Using VHDL",3rd Edition,Tata Mc Graw Hill,2009.**

OTHER REFERENCES	
1	**https://youtube.com/playlist?list=PLrkWJ9TJRalSSuRSF-ni9aPRZgQdPqdq-**
2	**https://youtu.be/NfXkffUivKQ**
3	**https://youtube.com/playlist?list=PLyqSpQzTE6M_dZdF7Bd-UncI5_L_1VkXF**
4	**https://youtu.be/aduM2zyf6p4**
5	**https://youtu.be/BeJOb6-Q904**

Semester	Programme	Course Code	Course Name	L	T	P	C
I	M.E. VLSI DESIGN	20MV1T3	CMOS VLSI DESIGN	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Explain and articulate the concepts of CMOS VLSI design	K2	1,2,3,4,5
CO2	Apply the concept of design in building VLSI Modules	K3	1,2,3,4,5
CO3	Compare the design to rate the performance combinational and sequential logic design	K4	2,3
CO4	Analyze the design to infer its limitations	K4	4,5
CO5	Evaluate the applications and recommend a suitable design to built a prototype	K5	5
CO6	Design a VLSI module for a given application	K6	5

PRE-REQUISITE	NIL

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	1										1	1
CO2	3	3	2	1									3	
CO3	3	1	2	2								1	3	
CO4	3	2	1	2					1				2	
CO5	3	2	2	1					1				2	
CO6	3	3	2	1									3	

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**MOS CIRCUIT DESIGN PROCESS**	**9**
Overview of VLSI Design Process - MOSFET Enhancement Transistors - MOS Physics - nFETCurrent-Voltage Equations - CMOS Inverter - DC Characteristics - Switching Characteristics - Dynamic Behavior-Power, Energy and Energy delay - Interconnects.		
Topic - 2	**COMBINATIONAL CMOS LOGIC DESIGN**	**9**
Static CMOS Design- Complementary CMOS- Pass Transistor Logic- Transmission Gate Logic -Dynamic CMOS Design- Signal Integrity Issues.		
Topic - 3	**SEQUENTIAL CMOS LOGIC DESIGN**	**9**
Static Latches and Registers - Dynamic Latches and Registers - Pulse Registers - Sense Amplifier based Registers - Pipelining – Non-bistable Sequential Circuits		
Topic - 4	**TIMING ISSUES IN VLSI CIRCUITS**	**9**
Timing Classification of Digital Systems - Timing Issues in Synchronous Design - Self Timed Circuit Design - Synchronizers and Arbiters.		
Topic - 5	**DESIGN OF ARITHMETIC BUILDING BLOCKS**	**9**
Datapaths in Digital Processor Architecture - Design of Adders: Binary Adder and Full Adder – Multiplier - Barrel and Logarithmic Shifters - Magnitude and Equality Comparators - Power and Speed Trade-offs in Datapath Structures		

THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	Jan M Rabaey, Anantha Chandrakasan and Borivoje Nikolic, "Digital Integrated Circuits - ADesign Perspective", 2nd Edition, Prentice Hall, 2012.
2	John P.Uyemura, "Introduction to VLSI Circuits and Systems", John Wiley & Sons, 2012.
3	Neil H. E. Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design - A Systems Perspective", 2nd Edition, Pearson Education, 2010.
4	Kamran Eshraghian, Douglas A. Pucknell, "Essentials of VLSI Circuits and Systems", PrenticeHall, 2011
5	C.Mead and L.Conway, "Introduction to VLSI Systems", Addison Wesley, 2003.
6	Kang, "CMOS Digital Integrated Circuits", McGraw Hill, 2002.

OTHER REFERENCES	
1	**https://youtu.be/oL8SKNxEaHs**
2	**https://youtu.be/faiEVOOCe-s**
3	**https://youtu.be/-AW9zksRuRE**
4	**https://youtu.be/vDqP4S4Jj1E**
5	**https://youtu.be/2t1M8ouI5pw**

Semester	Programme	Course Code	Course Name	L	T	P	C
I	M.E. VLSI DESIGN	20MV1T4	SYSTEM DESIGN USING FPGA	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Explain and articulate the concepts related to verilog HDL features and modelling	K2	1
CO2	Apply the types of PLD's and FPGA's in ASIC design	K3	2
CO3	Compare the FPGA systems and fabrics to rate its performance	K4	3
CO4	Analyze the combinational and sequential networks to infer its limitations	K4	4
CO5	Evaluate a situation based application and recommend a suitable FPGA architecture	K5	5
CO6	Design a FPGA prototype for a given application	K6	5

PRE-REQUISITE	NIL

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	1	2						1				1	1
CO2	3	3	2	1									3	
CO3	3	2	2									1	3	
CO4	3	2	1	1					1				2	
CO5	3	2	1	2					1				2	
CO6	3	2	2	1								1	3	

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**VERILOG HDL FEATURES AND MODELLING**	**9**
Overview of Digital design with Verilog HDL - Hierarchical Modelling Concepts -Lexical Conventions - Data types - Modules and Ports - Gate Level Modelling: Gate Types - Gate Delays - Data flow Modelling: Continuous Assignments - Expressions - Operator Types - Behavioural Modelling: Structures Procedures - Procedural Assignments - Conditional Statements - Multiway Branching - Loops - Tasks and Functions- Switch level Modelling -Design of combinational, sequential digital circuits using Verilog HDL.		
Topic - 2	**COMPLEX PROGRAMMABLE LOGIC DEVICES AND FGPAs**	**9**
Programmable Logic to ASICs - PROMS, PLAs, PALs, MGA ASICs, CPLDs and FPGAs - CPLDs – CPLD Architectures - Function Blocks - I/O Blocks - Clock Drivers - Interconnects - CPLD Technology and Programmable Elements - Embedded devices. FPGAs - FPGA Architectures - Configurable Logic Blocks - Configurable I/O Blocks – Programmable interconnects - Clock Circuitry - SRAM vs Antifuse Programming - Emulating and prototyping ASICs. Comparison of CPLDs and FPGAs.		
Topic - 3	**FPGA BASED SYSTEMS AND FABRICS**	**9**
Introduction - Basic Concepts - Digital Design and FPGAs - Role of FPGAs - FPGA Types - FPGA Based System Design - Registers and RAM. Introduction to FPGA Fabrics - FPGA Architectures - SRAM Based FPGAs - Permanently Programmed FPGAs - Chip I/O - Circuit Design of FPGA Fabrics - Architecture of FPGA Fabrics.		
Topic - 4	**COMBINATIONAL AND SEQUENTIAL LOGIC NETWORKS DESIGN**	**9**
Logic design Process - Modelling with HDLs - Combinational Network Delay - Power and Energy Optimization - Arithmetic Logic - Logic implementation for FPGAs - Physical Design for FPGAs - Sequential Machine Design Process - Sequential Design styles - Rules for Clocking - Performance analysis – Power Optimization.		
Topic - 5	**FPGA ARCHITECTURE DESIGN AND LARGE SCALE SYSTEMS**	**9**
Behavioural Design - Data path controller Architectures - Scheduling and Allocation - Power - Pipelining - Design Methodologies - Design Example - Digital Signal Processor. Introduction to Large scale systems - Busses - Platform FPGAs - Multi FPGA systems, Novel Architectures.		

THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	Samir Palnitkar, "Verilog HDL", 2nd Edition, Pearson Education, 2004.
2	Wayne Wolf, "FPGA- based System Design", Pearson Education, International Edition, 2004.
3	Bob Zeidman, "Designing with FPGAs and CPLDs, Elsevier, CMP Books, 2002.
4	Ion Grout, "Digital Systems Design with FPGAs and CPLDs", Elsevier, 2008.
5	Michael D. Ciletti, Advanced Digital Design with the Verilog HDL, 2nd Edition, Prentice Hall,2002
6	Charles H.Roth Jr "Digital Systems Design using VHDL", Cengage Learning, 2013.

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Semester	Programme	Course Code	Course Name	L	T	P	C
I	M.E. VLSI DESIGN	20MV1T5	DEVICE MODELLING AND SIMULATION	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Explain and articulate the concepts related to MOSFET device physics	K2	1
CO2	Apply the types of noise models in simulation	K3	2
CO3	Compare the other MOSFET models with BSIM4 models to rate its performance	K4	3
CO4	Analyze the mathematical techniques for simulation to infer its limitations	K4	4
CO5	Evaluate a situation based application and recommend a suitable modelling process for quality assurance	K5	5
CO6	Design a quality model prototype for a given application	K6	5

PRE-REQUISITE	NIL

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	1	2						1				1	1
CO2	3	3	2	1									3	
CO3	3	2	2									1	3	
CO4	3	1	1	2					1				2	
CO5	3	2	2	1					1				2	
CO6	3	2	2	2								1	3	

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**MOSFET DEVICE PHYSICS**	**9**
MOSFET capacitor, Basic operation, Basic modelling, Advanced MOSFET modelling, RF modelling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behaviour of MOS transistor and A.C small signal modelling, model parameter extraction, modelling parasitic BJT, Resistors, Capacitors, Inductors.		
Topic - 2	**NOISE MODELS AND BSIM4 MOSFET MODEL**	**9**
Noise sources in MOSFET-flicker noise modelling thermal noise modelling- BSIM4 MOSFET model-gate dielectric model-enhanced models for Effective dc and ac channel length and width-threshold voltage model-i-v model.		
Topic - 3	**OTHER MOSFET MODELS**	**9**
The EKV model, model features, long channel drain current model, modelling second order effects of the drain current, modelling of charge storage effects, Non- quasi-static modelling, noise temperature effects, MOS model 9, MOSAI model.		
Topic - 4	**MATHEMATICAL TECHNIQUES FOR DEVICE SIMULATIONS**	**9**
Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.		
Topic - 5	**MODELLING OF PROCESS VARIATION AND QUALITY ASSURANCE**	**9**
Influence of process variation, modelling of device mismatch for Analog/RF Applications, Benchmark circuits for quality assurance, Automation of the tests.		

THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	Philip E. Allen, Douglas R.Hoberg, ―CMOS Analog Circuit Design, Second Edition, Oxford Press-2002.
2	Trond Ytterdal, Yuhua Cheng and Tor A. Wayne Wolf, ―Device Modeling for Analog and RF CMOS Circuit Design, John Wiley & Sons Ltd.
3	Kiat Seng Yeo, Samir S. Rofail, Wang-Ling Gob, ―CMOS / BiCMOS CLSI Low Voltage Power‖, Person education low price edition2002
4	S.M.Sze, ―Semiconductor Devices –Physics and Technology, John Wiley and sons 1985.
5	Grasser, T., "Advanced Device Modeling and Simulation", World Scientific PublishingCompany., 2003.
6	Arora, N., "MOSFET Models for VLSI Circuit Simulation", Springer-Verlag, 1993.

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1	**https://youtu.be/zSVrTXHNbMQ**
2	**https://youtu.be/dyO5DPcL09g**
3	**https://youtu.be/HE-CXvevpBU**
4	**https://youtu.be/-6xN0iWOPrY**
5	**https://youtu.be/5KygwcZ545U**

Semester	Programme	Course Code	Course Name	L	T	P	C
I	M.E. VLSI DESIGN	20MV1E1	ADVANCED COMPUTER ARCHITECTURE AND PARALLEL PROCESSING	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Explain and articulate the concepts related to parallel processing, memory allocation in cache memories.	K2	1,2,3,4,5
CO2	Apply the types of parallel algorithm design using performance measures.	K3	2,4,5
CO3	Compare the parallelism in hardware/software to rate its performance.	K4	1,3,4
CO4	Analyze memory organization and mapping techniques to infer its limitations.	K4	3,4,5
CO5	Evaluate a situation based application and recommend a suitable modelling process for architectural features of advanced processors.	K5	4,5
CO6	Design different pipelined processors for a given application.	K6	3,4,5

PRE-REQUISITE	NIL

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	3	2								2		2
CO2	3	2	3		2					2		2		2
CO3	3	2	2	2	3									
CO4	3	2	2		2					2		2		
CO5	3	2	2	2	2					2		2		2
CO6	3	2	2	2	2					2		2		

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**PARALLEL PROCESSING, MEMORY AND I/O SUBSYSTEMS**	**9**
Generation of computer systems - Trends towards parallel processing - Parallel processing mechanisms Parallel computer structure - Architectural classification schemes - Hierarchical Memory structure - Virtual memory system - Cache memory management - Memory allocation and management - I/O subsystems.		
Topic - 2	**PIPELINING AND VECTOR PROCESSING**	**9**
Principles - Classification of pipeline processors - Reservation tables - Interleaved memory organization Design of arithmetic pipeline - Design of instruction pipeline - Basic vector processing architecture - Issues in vector processing - Vectorization and optimization methods.		
Topic - 3	**ARRAY PROCESSING**	**9**
SIMD Array processors - SIMD interconnection networks - Parallel algorithms for array processors - Associative array processing.		
Topic - 4	**MULTIPROCESSOR ARCHITECTURE**	**9**
Functional structures - Interconnection network - Multi cache problems and solutions - Exploiting concurrency for multiprocessing.		
Topic - 5	**PRINCIPLES OF PARALLEL ALGORITHM DESIGN**	**9**
Design approaches - Design issues-Performance measures and analysis - Complexities - Anomalies in parallel algorithms - Pseudo code conventions for parallel algorithms - Comparison of SIMD and MIMD algorithms.		

THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	**Philip E. Allen, Douglas R.Hoberg, —CMOS Analog Circuit Design, Second Edition, Oxford Press-2002.**
2	**Trond Ytterdal, Yuhua Cheng and Tor A. Wayne Wolf, —Device Modeling for Analog and RF CMOS Circuit Design, John Wiley & Sons Ltd.**
3	**Kiat Seng Yeo, Samir S. Rofail, Wang-Ling Gob, —CMOS / BiCMOS CLSI Low Voltage Power‖, Person education low price edition2002**
4	**S.M.Sze, —Semiconductor Devices –Physics and Technology, John Wiley and sons 1985.**
5	**Grasser, T., "Advanced Device Modeling and Simulation", World Scientific Publishing Company., 2003.**
6	**Arora, N., "MOSFET Models for VLSI Circuit Simulation", Springer-Verlag, 1993.**

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1	**https://youtu.be/NqgpZ_v4Ne8**
2	**https://youtu.be/uzECa-TZ0cw**
3	**https://youtu.be/aRN-uqSxgxs**
4	**https://youtu.be/EoONr6VZExA**
5	**https://youtu.be/o_n4AKwdfiA**

Semester	Programme	Course Code	Course Name	L	T	P	C
I	M.E. VLSI DESIGN	20MV1E2	SEMICONDUCTOR DEVICE MODELING	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Explain and articulate the concepts related to integrated diode and BJT.	K2	1,2,3,4,5
CO2	Apply the network equations to analyze the convergence and stability and use mathematical techniques for device simulations.	K3	2,3,5
CO3	Compare the knowledge of semiconductors to illustrate the functioning of basic electronic devices to rate its performance.	K4	2,3,4
CO4	Analyze amplification Application of the semiconductor devices to infer its limitations.	K4	1,4,5
CO5	Evaluate a fabrication method of integrated circuits of advanced processors.	K5	4,5
CO6	Design semiconductor devices for a given application.	K6	2,4,5

PRE-REQUISITE	NIL

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	3	3	2					3		2		2
CO2	3	2	3	2	2					3		3		2
CO3	3	2	3							2		2		
CO4	3	2	3							2				
CO5	3	3	3	3						3		3		2
CO6	3	2	2	2						2		3		

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**INTRODUCTION TO SEMICONDUCTOR PHYSICS & INTEGRATED PASSIVE DEVICES**	**9**
Review of Quantum Mechanics, Boltzmann transport equation. Continuity equation, Poisson equation. Types and Structures of resistors and capacitors in monolithic technology - dependence of model parameters on structure.		
Topic - 2	**INTEGRATED DIODES AND BIPOLAR TRANSISTOR**	**9**
Junction and Schottky diodes in monolithic technologies - static and dynamic behavior - small and large signal models - SPICE models.		
Topic - 3	**INTEGRATED MOS TRANSISTOR**	**9**
nMOS and pMOS Transistor - Threshold voltage - Threshold voltage equations - MOS device equations- Basic DC equations Second order effects - MOS models - Small signal AC Characteristics - MOSFET SPICE model level 1,2,3 and 4. \		
Topic - 4	**DEVICE MODELLING**	**9**
importance of circuit and device simulations in VLSI - Nodal, mesh, modified nodal and hybrid analysis equations - Solution of network equations - Sparse matrix techniques - solution of nonlinear networks through Newton-Raphson technique - convergence and stability.		
Topic - 5	**MATHEMATICAL TECHNIQUES FOR DEVICE SIMULATIONS**	**9**
Poisson equation - continuity equation - drift-diffusion equation - Schrodinger equation - hydrodynamic equations - trap rate, finite difference solutions to these equations in 1D and 2D space - grid generation.		

THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	**Sze S M, "Physics of Semiconductor Devices", 2nd Edition McGraw Hill, New York, 1981.**
2	**Tyagi M S, "Introduction to Semi-conductor Materials and Devices", John Wiley ,2003.**
3	**Tor A Fijedly, "Introduction to Device Modelling and Circuit Simulation", Wiley-Interscience, 1997.**
4	**Arora, N, "MOSFET Models for VLSI Circuit Simulation", Springer-Verlag, 1993.**
5	**Selberherr.S, "Analysis and Simulation of Semiconductor Devices", Springer-Verlag., 1984.**
6	**Grasser,T., "Advanced Device Modelling and Simulation", World Scientific Publishing Company, 2003.**

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1	**https://youtu.be/FHzx4Y1Gzf0**
2	**https://youtu.be/nV3bBrQnws0**
3	**https://youtu.be/rA-_oISKIQ8**
4	**https://youtu.be/I5Atvm3wRvg**
5	**https://youtu.be/MdpmhN8byvo**

Semester	Programme	Course Code	Course Name	L	T	P	C
I	M.E. VLSI DESIGN	20MV1E3	NANO ELECTRONICS	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Explain and articulate the concepts related to nano device fabrication technology.	K2	1,2,3,4,5
CO2	Apply the types of nano devices for memories using Data Transmission and Interfacing Displays.	K3	1,4,5
CO3	Compare the nano electronic devices to rate its performance.	K4	2,3,4
CO4	Analyze density of states / modes to infer its limitations.	K4	2,4,5
CO5	Evaluate a density of states / modes based application and recommend a suitable modelling process for architectural features of advanced processors.	K5	3,4,5
CO6	Design different density of states / modes for a given application.	K6	3,4,5

PRE-REQUISITE	NIL

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	3	3	3					3	3		2		2
CO2	2	3	3	3								2		2
CO3	3	2	3	3						2		2		
CO4	3	2	3	3					2					
CO5	3	2	3	3						2		2		2
CO6	2	3	3	3								2		

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT										
Topic - 1	**TECHNOLOGY AND ANALYSIS**									**9**
Dielectric, Ferroelectric and Optical properties - Film Deposition Methods - Lithography- Material removing techniques -Etchingand Chemical Mechanical Polishing -Scanning Probe Techniques.										
Topic - 2	**CARBON NANO STRUCTURES**									**9**
Principles and concepts of Carbon Nano tubes - Fabrication - Electrical, Mechanical and Vibration Properties - Applications of Carbon Nano tubes.										
Topic - 3	**LOGIC DEVICES**									**9**
Novel materials and alternative concepts - Single electron devices for logic applications - Super conductor digital electronics - Carbon Nano tubes for data processing.										
Topic - 4	**MEMORY DEVICES AND MASS STORAGE DEVICES**									**9**
Flash memories - Capacitor based Random Access Memories - Magnetic Random Access Memories - Information storage based on phase change materials - Resistive RandomAccess Memories - Holographic Data storage.										
Topic - 5	**DATA TRANSMISSION AND INTERFACING DISPLAYS**									**9**
Photonic Networks - RF and Microwave Communication System - Liquid Crystal Displays - Organic Light emitting diodes.										
THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	Rainer Waser, "Nano Electronics and Information Technology, Advanced Electronic materialsand novel devices", 3rd Edition, Wiley VCH, 2012.
2	T. Pradeep, "Nano: The essentials", Tata McGraw Hill, 2007.
3	Charles Poole, "Introduction to Nano Technology", Wiley Interscience, 2003.
4	C.Wasshuber Simon, "Simulation of Nano Structures Computational Single-Electronics",Springer, 2001.
5	Mark Reed and Takhee Lee, "Molecular Nano Electronics, American Scientific Publisher, California", 2003.
6	Vladimir V.Mitin, Viatcheslav A. Kochelap, Michael A. Stroscio, "Introduction to Nano Electronics Science, Nanotechnology, Engineering and Applications", Cambridge University Press, 2011.

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4	**https://youtu.be/r787m_IaR1I**

Semester	Programme	Course Code	Course Name	L	T	P	C
I	M.E. VLSI Design	20MV1L1	VLSI DESIGN LABORATORY I	0	0	3	1.5

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Design and simulate the CMOS digital and analog VLSI Circuits using Modern Tools, interface peripheral boards with FPGA, design layout of CMOS Circuits using back end tool and perform RTL synthesis using Xilinx Tool.	K3	1,2,3,4,5,6
CO2	Develop skills to communicate effectively	K2	1,2
CO3	Design layout of CMOS Circuits using back end tool Xilinx Tool	K3	8
CO4	Perform RTL synthesis using Xilinx Tool	K4	6
CO5	Design and simulation of FSM.	K5	2,5,6,7
CO6	Design of operational amplifiers	K5	9,10

PRE-REQUISITE	NIL

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	2	1	2		1					1		3
CO2	2	1	1										3	
CO3	2	1	2	1	3								2	
CO4	3	2	1	1	3									2
CO5	2	3	1	1	2									2
CO6	3	2	2	1	1								2	

COURSE ASSESSMENT METHODS		
DIRECT	1	Laboratory Record
	2	Model Practical Examinations
	3	End Semester Examinations
INDIRECT	1	Course End Survey

LIST OF EXPERIMENTS	
1	Writing Test benches using HDL for combinational and sequential circuits
2	Design and simulation of 4-bit barrel shifter using HDL
3	Design and simulation of 4-bit carry save adder using HDL
4	Design and simulation of Booth multiplier using HDL
5	Design and simulation of FSM using HDL
6	RTL Synthesis using Xilinx Tool
7	Design and Implementation of Matrix keyboard/ Stepper Motor controller using VHDL
8	IC Layout Design using EDA Tools (CMOS NOT, NAND & NOR Gates)
9	Design and simulation of differential amplifiers
10	Design and simulation of operational amplifiers

THEORY	0		TUTORIAL	0		PRACTICAL	45		TOTAL	45

BOOK REFERENCES	
1	**VLSI Lab Manual – I, Al-Ameen Publications, 2020.**
2	**John P.Uyemura, "Introduction to VLSI Circuits and Systems", John Wiley & Sons, 2012.**
3	**Neil H. E. Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design - A Systems Perspective", 2nd Edition, Pearson Education, 2010.**
4	**Kamran Eshraghian, Douglas A. Pucknell, "Essentials of VLSI Circuits and Systems", Prentice Hall, 2011**
5	**C.Mead and L.Conway, "Introduction to VLSI Systems", Addison Wesley, 2003.**

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SEMESTER II

Sl. No.	Course Code	Course Title	Category	CIA	ESE	L	T	P	C
	THEORY								
1	20MV2T1	Low power CMOS Circuits and Memories	PC	40	60	3	0	0	3
2	20MV2T2	Mixed Signal Circuit Design	PC	40	60	3	0	0	3
3	20MV2T3	Testing of VLSI Circuits	PC	40	60	3	0	0	3
4	20MV2T4	CAD for VLSI Circuits	PC	40	60	3	0	0	3
5	20MV2E1 to 20MV2E3	Professional Elective-II	PE	40	60	3	0	0	3
6	20MV2E4 to 20MV2E6	Professional Elective-III	PE	40	60	3	0	0	3
	LABORATORY								
7	20MV2L1	VLSI Design Laboratory – II	PC	60	40	0	0	3	1.5
8	20MV2L2	Mini project	EEC	100	--	0	0	3	1.5
Total						**18**	**0**	**6**	**21**

Semester	Programme	Course Code	Course Name	L	T	P	C
II	M.E. VLSI DESIGN	20MV2T1	LOW POWER CMOS CIRCUITS AND MEMORIES	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Illustrate the low power analysis of VLSI Circuits using various methods.	K2	1
CO2	Exemplify the basic and advanced memory technologies, types of memories and its reliability issues.	K3	1,2
CO3	Design and Analyze random access memory.	K4	2,3
CO4	Design the logic and circuit level low power circuits and impact of power on clock distribution.	K4	3,4
CO5	Design and Analyze FRAMs.	K5	4,5
CO6	Design and Analyze non volatile memory.	K5	3,4,5

PRE-REQUISITE	NIL

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	1	1			1		1	1	2			1	
CO2	2	1	1	1				1		1			1	
CO3	3	3	2	1		1	1		1	2		1		2
CO4	2	2	1	1			1				1	1		2
CO5	3	2	2	1		2		1	1			1		2
CO6	3	3	1	1			2	1	1	1		1		2

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**INTRODUCTION TO LOW POWER VLSI DESIGN AND POWER ANALYSIS METHODS**	**9**
Need for low power VLSI chips - Sources of power dissipation on Digital Integrated circuits - Physics of power dissipation in CMOS devices - Dynamic dissipation in CMOS - Technology impact on Low power- SPICE circuit simulators - Gate level logic simulation - Capacitive power estimation - Static state power - Gate level capacitance estimation		
Topic - 2	**CIRCUIT AND LOGIC LEVEL LOW POWER DESIGN AND CLOCK DISTRIBUTION**	**9**
Circuit level: Power consumption in circuits - Flip Flops and Latches design - High capacitance nodes - Low power digital cells library - Logic level: Gate reorganization - signal gating - logic encoding - state machine encoding - pre-computation logic. Power dissipation in clock distribution - Single driver Vs Distributed buffers - Zero skew Vs tolerable skew- Chip and package co-design of clock network.		
Topic - 3	**RANDOM ACCESS MEMORY TECHNOLOGIES**	**9**
SRAM cell structures - MOS SRAM Architecture and peripheral Circuit Operation - Advanced SRAM Architectures and Technologies - DRAM - CMOS DRAM - DRAM cell structures - BiCMOS DRAM - soft error failures in DRAM - Advanced DRAM Design and Architecture - Application Specific SRAMs and DRAMs		
Topic - 4	**NON-VOLATILE MEMORIES**	**9**
Masked ROMs - High Density ROMs - CMOS Programmable EPROMs - Floating Gate and One time Programmable ROMs - Electrically Erasable PROMS - Non volatile SRAM - Flash Memories - Advanced Flash Memory Architecture		
Topic - 5	**ADVANCED MEMORY TECHNOLOGIES AND ITS RELIABILITY ISSUES**	**9**
Ferroelectric Random Access Memories (FRAMs) - Gallium Arsenide (GaAs) FRAMs - Analog Memories- Magnetoresistive Random Access Memories (MRAMs) - Memory Cards. Reliability Issues: RAM Failure Modes and Mechanism - Nonvolatile Memory - Modelling and Failure Rate Prediction - Design for Reliability - Test Structures-Screening and Qualification		

THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	Gary K. Yeap ,Farid N. Najm, "Low power VLSI design and Technology", World Scientific Publishing Ltd., 1996.
2	Dimitrios Soudris, Christian Piguet, Costas Goutis, "Designing CMOS Circuits for LowPower", Kluwer Academic Publishers,2002.
3	Kaushik Roy , Sharat C. Prasad, "Low-Power CMOS VLSI Circuit Design", Wiley-Interscience, 2000
4	Ashok K Sharma, "Semiconductor Memories Technology, Testing and Reliability", Wiley,2002.
5	Etienne Sicard and Sonaia Delmas Bendhia, "Advanced CMOS Cell Design", Tata McGrawHill Publishing, 2007

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2	**https://www.youtube.com/watch?v=6XTYoZymbwE**
3	**https://www.youtube.com/watch?v=MP6VlAE_7WY**

Semester	Programme	Course Code	Course Name	L	T	P	C
II	M.E. VLSI DESIGN	20MV2T2	MIXED SIGNAL CIRCUIT DESIGN	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Analyze and Design submicron CMOS circuits.	K2	1
CO2	Analyze and Design switched capacitor circuits.	K3	1,2
CO3	Analyze of Nonlinearity circuits.	K4	2,3
CO4	Analyze and Design of continuous time filters.	K4	3,4
CO5	Design of Digital to Analog converters.	K3	4,5
CO6	Design of Oscillators and PLLs.	K3	3,4,5

PRE-REQUISITE	NIL

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	2	1	1		1		2		1		1		2
CO2	2	2	1	1	1		2		1		1			1
CO3	3	2	1	1		1		1		1	1	1		2
CO4	2	2	1	1	1		2	1	1				2	
CO5	2	1	2	1		2	1	2	1		1	1	2	
CO6	2	1	1	1	2	1	1			1	1	1	1	

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**SUBMICRON CMOS CIRCUIT DESIGN**	**9**
CMOS Process flow - Capacitors and resistors -Digital circuit design: MOSFET switch - Delay elements - adder- Analog circuit design: Biasing - Op amp Design - Mixed-Signal Layout Issues: Floor Planning- Power Supply and Grounding Issues- Fully Differential Design- Guard Rings- Shielding –Interconnect		
Topic - 2	**CONTINUOUS TIME FILTERS**	**9**
First order filters-Second order filters- Gm-C filters- Transconductors Using Fixed Resistors- CMOS Transconductors Using Triode Transistors- CMOS Transconductors Using Active Transistors- Bipolar Transconductors - Bicmos Transconductors - Active RC And MOSFET-C Filters- Tuning Circuitry- Complex Filters		
Topic - 3	**NONLINEARITY AND SWITCHED CAPACITOR CIRCUITS**	**9**
Basic building blocks - Basic operation and analysis - Noise in Switched Capacitor Circuits - First-Order Filters - Biquad Filters- Charge Injection- Switched Capacitor Gain Circuits- Correlated Double-Sampling Techniques- Switched capacitor amplifiers - Switched capacitor integrator - Nonlinearity – Mismatch		
Topic - 4	**DIGITAL TO ANALOG AND ANALOG TO DIGITAL CONVERTERS**	**9**
Introduction and characterization of DAC - Parallel DAC - Extending the resolution of parallel DAC - Serial DAC - Introduction and characterization of ADC - Serial ADC - Medium ADC - High speed ADC		
Topic - 5	**OSCILLATORS AND PLLs**	**9**
Oscillatory system - Ring oscillators - LC oscillators - Voltage Controlled Oscillators (VCO) - Mathematical model of VCO - Simple PLL - Charge pump PLLs - Non ideal effects in PLLs: PFD/CP non idealities - jitter in PLLs - Delay locked loops - PLL applications		

THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	B. Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2002
2	R.J. Baker, "CMOS Mixed-Signal Circuit Design", Wiley Publications, 2002
3	R.J. Baker, H.W. Li, D.E. Boyce, "CMOS Circuit design, Layout, and Simulation", Wiley-IEEEPress, 3rd Edition, 2010
4	Tony Chan Carusone, David A. Johns and Ken Martin, "Analog Integrated Circuit Design",John Wiley and Sons, 2nd Edition, 2011
5	Phillip E.Allen and Douglas R.Holberg, "CMOS Analog Circuit Design", Oxford UniversityPress, 2002

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1	**https://www.youtube.com/watch?v=_nEt8ZONlPI**
2	**https://www.youtube.com/watch?v=C4zctTkPxxw**
3	**https://www.allaboutcircuits.com/technical-articles/what-is-mixed-signal-ic-design/**

Semester	Programme	Course Code	Course Name	L	T	P	C
II	M.E. VLSI DESIGN	20MV2T3	TESTING OF VLSI CIRCUITS	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Design of Testing and Fault Modelling.	K3	1
CO2	Analyze and Design of Testable Sequential Circuits.	K4	1,2
CO3	Analyze and Design of Testable Combinational circuits.	K4	2,3
CO4	Verify Test Algorithms.	K4	3,4
CO5	Design of Fault Diagnosis for Combinational Circuits.	K3	4,5
CO6	Design for Testability.	K4	3,4,5

PRE-REQUISITE	NIL

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	1	1		1			1		1		2	
CO2	3	2	1	1	1			1		1	2		2	
CO3	2	2	2	1								1	2	
CO4	3	1	1	1	2	1		1		1	1			2
CO5	3	2	1	2	1				1		2			2
CO6	3	2	1	1						1	1	1	2	

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**BASICS OF TESTING AND FAULT MODELLING**	**9**
Introduction to Testing - Faults in Digital Circuits - Modelling of faults - Logical Fault Models - Fault detection - Fault Location - Fault dominance - Logic simulation - Types of simulation - Delay models - Gate Level Event-driven simulation.		
Topic - 2	**TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS**	**9**
Test generation for Combinational logic circuits - Testable Combinational logic circuit design - Test generation for Sequential circuits - Design of Testable sequential circuits		
Topic - 3	**DESIGN FOR TESTABILITY**	**9**
Design for Testability - Ad-hoc design - Generic Scan based design - Classical scan based design - System level DFT approaches.		
Topic - 4	**SELF - TEST AND TEST ALGORITHMS**	**9**
Built-in self Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test Algorithms - Test generation for Embedded RAMs.		
Topic - 5	**FAULT DIAGNOSIS**	**9**
Logical Level Diagnosis - Diagnosis by Unit Under Test reduction - Fault Diagnosis for Combinational Circuits - Self checking design - System level Diagnosis		

THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	M.Abramovici, M.A.Breuer and A.D. Friedman, "Digital systems and Testable Design", Jaico Publishing House, 2002.
2	P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002
3	M.L.Bushnell ,V.D.Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2002.
4	A.L.Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice HallInternational, 2002

OTHER REFERENCES	
1	**https://www.youtube.com/watch?v=MP6VlAE_7WY**
2	**https://www.youtube.com/watch?v=6XTYoZymbwE**

Semester	Programme	Course Code	Course Name	L	T	P	C
II	M.E. VLSI DESIGN	20MV2T4	CAD FOR VLSI CIRCUITS	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Outline the VLSI design Methodologies; apply the algorithms for VLSI Automation.	K3	1
CO2	Explain and evaluate the various physical design concepts, simulation and high level synthesis issues in CAD of VLSI.	K3	1,2
CO3	Design advanced electronics systems.	K4	2,3
CO4	Evaluate and analyze the systems in VLSI design environments.	K4	3,4
CO5	Apply advanced technical knowledge in multiple contexts.	K3	4,5
CO6	Conduct an organized and systematic study on significant research topic within the field of VLSI and its allied field.	K4	3,4,5

PRE-REQUISITE	NIL

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	1	1	1	1				2	1			1	2
CO2	3	2	1	1	1	1			1		1		2	
CO3	3	2	1	1			1	1		1				2
CO4	3	2	1			1	1				1			2
CO5	3	2	1				1		1	1			1	
CO6	3	2	1	1		1		1			1	2		1

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**INTRODUCTION TO VLSI DESIGN METHODOLOGIES**	**9**
VLSI Design Cycle - Physical Design Cycle - Design Styles and comparison of different Design Styles Fabrication of VLSI Circuits		
Topic - 2	**VLSI DESIGN AUTOMATION**	**9**
VLSI Design Automation Tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable Problems - General Purpose Methods for Combinational Optimization - Back tracking and Branch and Bound - Local Search - Simulated annealing and genetic algorithms.		
Topic - 3	**PHYSICAL DESIGN**	**9**
Layout Compaction - Placement and Partitioning - Circuit Representation - placement algorithms - Partitioning - Floor Planning Concepts - Shape Functions and Floor Planning Sizing - types of local routing problems - Area Routing - Channel Routing - Global Routing.		
Topic - 4	**SIMULATION AND SYNTHESIS**	**9**
Simulation - Gate Level Modelling and Simulation - Switch Level Modelling and Simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.		
Topic - 5	**HIGH LEVEL SYNTHESIS**	**9**
Hardware Models - Internal Representation - Allocation assignment and scheduling - Simple Scheduling Algorithm - Assignment Problem.		

THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	S.H.Gerez, "Algorithms for VLSI Design Automation", John Wiley and Sons, 2002.
2	N.A.Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwar AcademicPublishers, 2002
3	Drechsler,R., "Evolutionary Algorithms for VLSI CAD", Kluwer Academic Publishers,Boston,1998
4	Glyn James., “Advanced Modern Engineering Mathematics”, Pearson Education Limited,2007.
5	Hill,D.D.Shugard, J. Fishburn and K. Kuetzer, "Algorithms and Techniques for VLSI Layout Synthesis", Kluwer Accademic Publishers, Boston, 1989.

OTHER REFERENCES	
1	**https://www.youtube.com/watch?v=MP6VlAE_7WY**
2	**https://www.youtube.com/watch?v=6XTYoZymbwE**

Semester	Programme	Course Code	Course Name	L	T	P	C
II	M.E. VLSI DESIGN	20MV2E1	SIGNAL INTEGRITY FOR HIGH SPEED DEVICES	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	To Apply the concepts of Signal Integrity in Electromagnetic Fields	K3	1
CO2	To Analyse the Inductance and Capacitance values in Signal Propagation.	K4	2
CO3	To Analyse the characteristics of Dielectric material in Signal Propagation	K4	3
CO4	To Analyse the characteristics of noise models in Signals	K4	4
CO5	To evaluate the different model of Physical transmission line.	K5	5
CO6	To Design the new methods to improve the signal transmission characteristics	K6	5

PRE-REQUISITE	20MV2T2 - Mixed Signal Circuit Design

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	2	2	2					3				3
CO2	2	3	2	2			2			3	3			3
CO3	2	3	2	2	1			2		2				2
CO4	1	3	2	2			2			1	3			2
CO5	2	2	3	2	1					2				1
CO6	1	2	2	3		3				2				3

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**SIGNAL INTEGRITY**	**9**
The importance of signal integrity - new realm of bus design - Electromagnetic fundamentals for signal integrity - Maxwell equations common vector operators - wave propagations - Electrostatics - magneto statics - Power flow and the poynting vector - Reflections of electromagnetic waves.		
Topic - 2	**CROSS TALK**	**9**
Introduction - mutual inductance and capacitance-coupled wave equation - coupled line analysis - modal analysis - cross talk minimization signal propagation in unbounded conductive media - classic conductor model for transmission model.		
Topic - 3	**DI-ELECTRIC MATERIALS**	**9**
Polarization of Dielectric - Classification of Dielectric material - frequency dependent dielectric material - Classification of Dielectric material fiber - Wave effect - Environmental variation in dielectric behavior Transmission line parameters for loose dielectric and realistic conductors		
Topic - 4	**DIFFERENTIAL SIGNALING**	**9**
Removal of common mode noise - Differential Cross talk - Virtual reference plane-Propagation of model voltages common terminology - drawbacks of differential signalling.		
Topic - 5	**PHYSICAL TRANSMISSION LINE MODEL**	**9**
Introduction - non ideal return paths - Vias - IO design consideration - Push-pull transmitter - CMOS receivers - ESSD protection circuits - On chip Termination		

THEORY	**45**	**TUTORIAL**	**0**	**PRACTICAL**	**0**	**TOTAL**	**45**

BOOK REFERENCES	
1	Stephen H. Hall, Howard L. Heck, "Advanced Signal Integrity for High-Speed DigitalDesigns", Wiley IEEE Press, 2009.
2	James Edgar Buchanan, "Signal and power integrity in digital systems: TTL, CMOS, and BiCMOS ", Mc Graw Hill,1996.
3	Greg Edlund, "Timing Analysis and Simulation for Signal Integrity Engineers", Prentice Hallof India, 2008
4	Stephen C. Thierauf, "Understanding Signal Integrity", Pages displayed by permission Artech Publishing House, 2011.
5	Eric Bogatin, "Signal and Power Integrity - Simplified", 2nd Edition, Prentice Hall of India,2010
6	Mike Peng Li, "Jitter, Noise and Signal Integrity at High-Speed", Prentice Hall of India, 2008.

OTHER REFERENCES	
1	**https://www.youtube.com/watch?v=oxrXfIimy_Q**
2	**https://www.youtube.com/watch?v=TExobD7vDUY**
3	**https://www.youtube.com/watch?v=anX8QZMhVjI**
4	**https://www.youtube.com/watch?v=A6W5A8L9vu8**
5	**https://www.youtube.com/watch?v=ZFYESaEE5D0**

Semester	Programme	Course Code	Course Name	L	T	P	C
II	M.E. VLSI DESIGN	20MV2E2	HIGH SPEED DIGITAL DESIGN	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	To understand the concepts of Transmission Lines and Crosstalk in signal propagation	K2	1
CO2	To analyse the inductance and capacitance values in Transmission Lines	K4	2
CO3	To evaluate the Synchronization of clock signals	K5	3
CO4	To analyse the noise level and cross talk in signal transmission	K4	4
CO5	To analyse the ground systems in signal transmission	K4	5
CO6	To design a new model of high speed transmission lines without any losses	K6	5

PRE-REQUISITE	20MV1T2 - Advanced Digital System Design

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	2	2	2	2					3				3
CO2	2	3	2	2			2			3	3			3
CO3	2	2	3	2	1			2		2				2
CO4	1	3	2	2			2			1	3			2
CO5	2	3	2	2	1					2				1
CO6	1	2	2	3		3				2				3

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**TRANSMISSION LINES AND CROSSTALK**	**9**
Transmission line structures, signal propagation, transmission line parameters, line impedance, propagation delay, Transmission line reflections, Cross talk- Mutual inductance, Mutual capacitance, cross talk induced noise, minimizing cross talk		
Topic - 2	**POWER DISTRIBUTION**	**9**
Losses, the need for low-impedance planes and decoupling capacitors and their selection.		
Topic - 3	**CLOCK DISTRIBUTION AND TIMING**	**9**
High-quality clock signals to components - boards and systems - Common clock timing and source synchronous timing		
Topic - 4	**INTERCONNECTS & ELECTROMAGNETIC COMPATIBILITY (EMC)**	**9**
Interconnect technologies - Multilevel multilayer interconnects - propagation delay - crosstalk analysis - Designing for EMC - EMC regulations - typical noise path - methods of noise coupling - methods of reducing interference in systems.		
Topic - 5	**GROUNDING**	**9**
Safety grounds ,signal grounds, single-point ground systems, multi-point ground systems, hybrid grounds, functional ground layout, practical low frequency grounding, hardware grounds, grounding of cable shields, ground loops, shield grounding at high frequencies		

THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	Howard Johnson, Martin Graham, "High speed Digital design", Pearson, 2005
2	Hall S, Hall G and McCall J, "High Speed Digital System Design: A Handbook of Interconnect Theory and Practices", Wiley Interscience,2000.
3	Hartmut Grabinski, " Interconnects in VLSI design", Kluwer, 2000.
4	Goel A K , "High speed VLSI interconnections", Wiley 2007.
5	Bogatin E, "Signal integrity-simplified", Prentice Hall, 2003
6	Paul CR, "Introduction t Electromagnetic compatibility", Wiley 2006.

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1	**http://www.digimat.in/nptel/courses/video/117106089/L36.html**
2	**https://nptel.ac.in/courses/117/106/117106089/**
3	**http://www.nptelvideos.in/2012/12/high-speed-devices-circuit.html**
4	**https://www.digimat.in/nptel/courses/video/117106089/L01.html**

Semester	Programme	Course Code	Course Name	L	T	P	C
II	M.E. VLSI DESIGN	20MV2E3	DSP INTEGRATED CIRCUITS	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	To understand the concepts of DSP and DSP algorithms	K2	1,2
CO2	To Analyze Multirate systems and finite word length effects	K4	3
CO3	To Analyze the filters Specifications in DSP Processors	K4	3
CO4	To Analyze the basic DSP processor architectures and the synthesis of the processing elements	K4	4
CO5	To evaluate the numbering systems in DSP Processors	K5	5
CO6	To Design a new DSP algorithms for different input numbering system	K6	5

PRE-REQUISITE	NIL

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	2	2	2	2					3				3
CO2	2	3	2	2			2			3	3			3
CO3	2	3	2	2	1			2		2				2
CO4	1	3	2	2			2			1	3			2
CO5	2	2	3	2	1					2				1
CO6	1	2	2	3		3				2				3

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**DSP INTEGARTED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES**	**9**
Standard digital signal processors - Application specific IC's for DSP - DSP systems - DSP system design - Integrated circuit design - MOS transistors - MOS logic - VLSI process technologies		
Topic - 2	**DIGITAL SIGNAL PROCESSING**	**9**
Digital signal processing - Sampling of analog signals - Selection of sample frequency - Signal processing systems - Frequency response - Transfer functions - Signal flow graphs - Filter structures- Adaptive DSP algorithms - DFT - FFT - Image coding - Discrete cosine transforms.		
Topic - 3	**DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS**	**9**
FIR filters - FIR filter structures - IIR filters - Specifications of IIR filters - Mapping of analog transfer functions - Mapping of analog filter structures - Multirate systems - Interpolation with an integer factor L Sampling rate change with a ratio L/M - Multirate filters - Finite word length effects - Parasitic oscillations - Scaling of signal levels - Roundoff noise - Measuring round-off noise - Coefficient sensitivity - Sensitivity and noise		
Topic - 4	**DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES**	**9**
DSP system architectures - Ideal DSP architectures - Multiprocessors and multicomputers - Systolic and Wave front arrays - Shared memory architectures - Mapping of DSP algorithms onto hardware - Implementation based on complex PEs - Shared memory architecture with Bit - serial PEs..		
Topic - 5	**NUMBER SYSTEMS - ARITHMETIC UNITS AND INTEGARTED CIRCUIT DESIGN**	**9**
Conventional number system - Redundant Number system - Residue Number System - Bit-parallel and Bit-Serial arithmetic - Basic shift accumulator - Reducing the memory size - Complex multipliers - Layout of VLSI circuits		

THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	Lars Wanhammer, "DSP Integrated Circuits", Academic press, New York, 1999.
2	Barrett Hazeltine, Lars Wanhammar, Christopher Bull, "Appropriate Technology: Tools,Choices and Implications, Academic Publishers, 1999
3	A.V. Oppenheim et.al, "Discrete-time Signal Processing", Pearson Education, 2000
4	Keshab K.Parhi, "VLSI digital Signal Processing Systems design and Implementation",JohnWiley & Sons, 1999
5	Emmanuel C. Ifeachor, Barrie W. Jervis, "Digital Signal Processing, A Practical Approach", 2nd Edition, Prentice Hall, 2001
6	K. Padmanabhan, S. Anandhi, R. Vijayarajeswaran "A Practical Approach to Digital Signal Processing", New Age International, 2001

OTHER REFERENCES	
1	**https://www.youtube.com/watch?v=tvOF1wIL7dw**
2	**https://www.youtube.com/watch?v=vcCpeNeavUM**
3	**https://www.youtube.com/watch?v=Iw77CYUT74c**
4	**https://www.youtube.com/watch?v=a4C5vpiBm4Q**
5	**https://www.youtube.com/watch?v=03j4ZvQCKWY&list=PL36E832F4CA46D233**

Semester	Programme	Course Code	Course Name	L	T	P	C
II	M.E. VLSI DESIGN	20MV2E4	ASIC DESIGN	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Describe the design flow, types and the programming technologies of an ASIC and its construction.	K1	1
CO2	Ability to know ASIC interconnects, design software, synthesize andconstruct ASICs.	K2	2
CO3	Understand the basics of ASIC design flow and library design.	K2	3
CO4	Gain a well founded knowledge of logical cells and i/o cells.	K3	4
CO5	Apply various logic synthesis techniques, simulation and testing in digital system design.	K5	5
CO6	Implement the ASIC construction, floor planning, placement and routing.	K4	4,5

PRE-REQUISITE	NIL

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	1							1				1	
CO2	3	1	1	1	1							2	1	
CO3	3	2	1	1					1				1	
CO4	3	1							1				1	
CO5	3	1	2	1	1								1	
CO6	3	2	1	1								1	1	

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**FUNDAMENTALS OF ASICs, CMOS LOGIC AND ASIC LIBRARY DESIGN**	**9**
Types of ASICs - Design flow-CMOS Transistors CMOS Design Rules - Combinational Logic Cell - Sequential Logic cell - Data path Logic Cell -Transistors as Resistors -Transistor Parasitic Capacitance- Logical effort - Library Cell Design-Library Architecture.		
Topic - 2	PROGRAMMABLE ASICs	**9**
Anti fuse - Static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA - Altera FLEX - Altera MAX DC and AC inputs and outputs - Clock and Power inputs - Xilinx I/O blocks		
Topic - 3	PROGRAMMABLE ASIC INTERCONNECT, DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY	**9**
Actel ACT - Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX - Design Systems - Logic Synthesis - Half gate ASIC - Schematic entry - Low level design language - PLA tools - EDIF-CFI design representation		
Topic - 4	LOGIC SYNTHESIS - SIMULATION AND TESTING	**9**
Verilog and Logic Synthesis -VHDL and Logic Synthesis - Types of Simulation - Boundary Scan Test - Fault simulation - Automatic Test Pattern Generation.		
Topic - 5	ASIC CONSTRUCTION	**9**
System partition - FPGA partitioning - Partitioning methods - Floor planning - placement - Physical Design Flow - Global Routing - Detailed Routing - Special Routing - Circuit extraction – DRC.		

THEORY	**45**		**TUTORIAL**			**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	Smith M.J.S.,"Application Specific Integrated Circuits", Addison, Wesley Longman Inc.,1997.
2	Farzad Nekoogar and Faranak Nekoogar, "From ASICs to SoCs - A Practical Approach", Prentice Hall, 2003
3	Rajsuman R., "System-on-a-Chip Design and Test", Santa Clara, CA, Artech HousePublishers, 2000.
4	Wayne Wolf, "FPGA-Based System Design", Prentice Hall, 2004
5	Nekoogar F.,"Timing Verification of Application-Specific Integrated Circuits", Prentice Hall,1999

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2	**https://youtu.be/QP-4FlwNTvw**
3	**https://youtu.be/5fESTph5gA8**
4	**https://youtu.be/mZItfJIEFMk**
5	**https://youtu.be/t3thKRqMK2M**

Semester	Programme	Course Code	Course Name	L	T	P	C
II	M.E VLSI DESIGN	20MV2E5	MICROSENSORS AND MEMS	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Ability to understand the operation of micro devices, micro systems and their applications.	K2	1
CO2	Ability to design the micro devices, micro systems using the MEMS fabrication process.	K3	2
CO3	Gain knowledge of basic approaches for various sensor designs.	K3	3
CO4	Gain a knowledge of basic approaches for various actuator design	K3	4
CO5	Develop experience on micro system for photonics	K4	5
CO6	Gain the technical knowledge required for computer-aided design, fabrication, analysis and characterization of nano-structured materials, micro- and nano-scale devices.	K4	1,2,3,4,5

PRE-REQUISITE	NIL

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	1							1				1	
CO2	3	1										2	1	
CO3	3	2	1	1					1				1	
CO4	3	1							1				1	
CO5	3	1											1	
CO6	3	2	1	1								1	1	

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**MEMS AND MICROSYSTEMS**	**9**
MEMS and Microsystems - Evaluation of micro fabrication - micro-systems and microelectronics - applications - working principles of Microsystems - micro-sensors - micro actuators - micro accelerometers- Scaling Laws In Miniaturization - scaling in geometry, rigid body dynamics, trimmer force, electrostatic forces, Electromagnetic forces, electricityand fluidic dynamics and heat -conductingand heat convection.		
Topic - 2	**MATERIALS FOR MEMS AND MICROSYSTEMS**	**9**
Substrates and wafers - silicon as a substrate material - Ideal substrates for MEMS - single crystal silicon and wafers crystal structure - mechanical properties of Si, silicon compounds, SiO2, SiC, Si3N4 and polycrystalline Silicon - silicon piezo resistors, gallium arsenide, quartz, piezoelectric crystals - polymers for MEMS - conductive polymers.		
Topic - 3	**MICRO SENSORS**	**9**
Introduction to micro-sensors - biomedical sensors - pressure sensors - thermal sensors - chemical sensors - moptical sensors - micro-actuation - MEMS with micro actuators.		
Topic - 4	**ENGINEERING MECHANICS FOR MICROSYSTEMS DESIGN**	**9**
Static bending of thin plates - circular plates with edge fixed - rectangular plates with all edges fixed and square plates with all edges fixed - Mechanical vibration - resonant vibration - micro accelerometers - design theory of damping coefficients - Thermo mechanics - thermal stresses - Fracture mechanics - stress intensity factors - fracture toughness and interfacial fracture machine.		
Topic - 5	**MICROSYSTEM DESIGN**	**9**
Design considerations - design constraints - selection of materials - manufacturing process - signal transduction - packaging - process design - photolithography - Thin film fabrications - geometry shaping mechanical design - design of silicon die for micro-pressure sensor		

THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	Tai Ran Hsu, "MEMS & Micro systems Design, Manufacture and Nano scale Engineering"John Wiley and sons, New Jersey, 2nd Edition, 2008
2	Chang Liu, "Foundation of MEMS", Pearson Edition, 2nd Edition ,2011
3	Stephen Beeby, Graham Ensell, "MEMS, Mechanical Sensors", Artech House Publishers, 2004.
4	Wanjun Wang, Steven A. Soper," Bio-MEMS Technologies and Applications", CRC Press,2007.
5	Sergey Edward Lyshevski, "Nano and Micro Electro Mechanical System", CRC Press, 2001

OTHER REFERENCES	
1	**https://youtu.be/t3thKRqMK2M**
2	**https://youtu.be/TtAsMwhVcAs**
3	**https://youtu.be/QVBgKAZIvpI**
4	**https://youtu.be/98gmOUItrPk**
5	**https://youtu.be/0PLyBaZ6MCU**

Semester	Programme	Course Code	Course Name	L	T	P	C
II	M.E. VLSI DESIGN	20MV2E6	ADVANCED EMBEDDED SYSTEM DESIGN	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Explain and articulate the basic concepts related to embedded hardware.	K2	1,3
CO2	Apply the Real time operating system in embedded system	K3	2
CO3	Compare hardware and software relation and rate to their performance of peripherals.	K4	3
CO4	Analyse the memory and interfacing of embedded system	K4	4
CO5	Evaluate the situation based on concurrent process model and hardware, software co design to an embedded system.	K5	3,5
CO6	Design a embedded equipment for given application	K6	2,3,4

PRE-REQUISITE	NIL

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	2											2	2
CO2	3	2	3		3						2		2	
CO3	2	2				2								
CO4	3		2					2					2	
CO5	2	2	3				1						2	
CO6		2	2	2							2		2	

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**INTRODUCTION TO EMBEDDED HARDWARE**	**9**
Terminology - Gates - Timing diagram - Memory - Microprocessor buses - Direct memory access Interrupts- Built interrupts - Interrupts basis - Shared data problems - Interrupt latency - Embedded system evolution trends - Round robin - Round robin with interrupt function - Rescheduling architecture - algorithm		
Topic - 2	**REAL TIME OPERATING SYSTEM**	**9**
Task and Task states - Task and data - Semaphore and shared data operating system services - Message queues timing functions - Events - Memory management - Interrupt routines in an RTOS environment - Basic design using RTOS		
Topic - 3	**EMBEDDED HARDWARE, SOFTWARE AND PERIPHERALS**	**9**
Custom single purpose processors: Hardware - Combination Sequence - Processor design - RT level design - optimizing software: Basic Architecture - Operation - Programmers view - Development Environment - ASIP - Processor Design - Peripherals - Timers, counters and watch dog timers - UART - Pulse width modulator - LCD controllers - Key pad controllers - Stepper motor controllers - A/D converters- Real time clock		
Topic - 4	**MEMORY AND INTERFACING**	**9**
Memory: Memory write ability and storage performance - Memory types - Composing memory Advance RAM interfacing communication basic - Microprocessor interfacing I/O addressing Interrupts - Direct memory access - Arbitration multilevel bus architecture - Serial protocol - Parallel protocols - Wireless protocols - Digital camera example..		
Topic - 5	**CONCURRENT PROCESS MODELS AND HARDWARE SOFTWARE CO - DESIGN**	**9**
Modes of operation - Finite state machines - Models - HCFSL and state charts language - State machine models - Concurrent process model - Concurrent process -Communication among process - Synchronization among process - Implementation - Data Flow model. Design technology - Automation synthesis - Hardware software co - simulation - IP cores - Design Process Model.		

THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	Steve Heath, "Embedded System Design", 2nd Edition, Newnes Publications, 2004.
2	Frank Vahid and Tony Gwargie, "Embedded System Design", 3rd Edition ,John Wiley & sons,2009.
3	David E Simon, "An Embedded Software Primer", Pearson Education Asia, 7th Edition, 2009.
4	Rajkamal, "Embedded Systems: Architecture, Programming and Design", 2nd Edition, Tata McGraw- Hill, 2008
5	Arnold Berger, "Embedded System Design: An Introduction to Processes, Tools, and Techniques", CMP Books, 1st Edition, 2002.

OTHER REFERENCES	
1	**https://youtu.be/MfhTBeaDpQA**
2	**http://www.brown.edu/Departments/Engineering/Labs/ddzo/async.html**
3	**https://youtu.be/7LqPJGnBPMM**
4	**https://youtu.be/TP1_F3IVjBc**
5	**https://youtu.be/84YUQu8tE4w**

Semester	Programme	Course Code	Course Name	L	T	P	C
II	M.E. VLSIDESIGN	20MV2L1	VLSI DESIGN LABORATORY II	0	0	3	1.5

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Perform power analysis, simulate the Memories using HDL and EDA Tools, design filters, simulate the CMOS Circuits in back end and analyze the interconnect issues in VLSI Circuits.	K2	1
CO2	Develop skills to communicate effectively	K3	2,3,4
CO3	Acquire knowledge about digital system design and implementation in FPGAs	K3	5,6
CO4	Analysis knowledge of various parameters by T-SPICE tool.	K5	7
CO5	Design and implement the Embedded systems.	K5	8
CO6	Acquire knowledge of layout level design entries.	K4	9,10

PRE-REQUISITE	NIL

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	2	2	2		1		1				2	2
CO2	3	2	2	1	2		1					1	1	
CO3	3	2	1	1	2		1		1			1	2	
CO4	3	2	1	1	1		1					1	2	
CO5	3	1	1	1	1		1					1	2	
CO6	3	2	1	1	1		1					1	2	

COURSE ASSESSMENT METHODS		
DIRECT	1	Laboratory Record
	2	Model Practical Examinations
	3	End Semester Examinations
INDIRECT	1	Course End Survey

LIST OF EXPERIMENTS	
1	Design and simulation of ADC
2	Power analysis of Digital Circuits using HDL
3	Design and Simulation of ROM and RAM model using HDL
4	Design and Simulation of analog filters
5	Fault Simulation and Fault Diagnosis of digital circuits
6	Event Driven Simulation for gate level combinational circuits
7	Design and Simulation of CMOS Digital Circuits using EDA tools
8	Design and Simulation of SRAM and DRAM using EDA Tools
9	Implementation of Task Scheduling and Placement Algorithms
10	Interconnects in VLSI circuits

THEORY	0		TUTORIAL	0		PRACTICAL	45		TOTAL	45

BOOK REFERENCES	
1	VLSI Lab Manual - II, Al-Ameen Publications, 2020.
2	Neil H.E. Weste, David Money Harris —CMOS VLSI Design: A Circuits and SystemsPerspective‖, 4th Edition, Pearson , 2017
3	Jan M. Rabaey ,Anantha Chandrakasan, Borivoje. Nikolic, ‖Digital Integrated Circuits:ADesign perspective‖, Second Edition , Pearson , 2016.

OTHER REFERENCES	
1	**M.J. Smith, —Application Specific Integrated Circuits‖, Addisson Wesley, 1997**
2	**Sung-Mo kang, Yusuf leblebici, Chulwoo Kim —CMOS Digital Integrated Circuits:Analysis & Design‖,4th edition McGraw Hill Education,2013**
3	**Wayne Wolf, —Modern VLSI Design: System On Chip‖, Pearson Education, 2007**
4	**R.Jacob Baker, Harry W.LI., David E.Boyee, —CMOS Circuit Design, Layout and Simulation‖, Prentice Hall of India 2005.**

SEMESTER III

Sl. No.	Course Code	Course Title	Category	CIA	ESE	L	T	P	C
	THEORY								
1	20MV3E1 to 20MV3E3	Professional Elective-IV	PE	40	60	3	0	0	3
2	20MV3E4 to 20MV3E6	Professional Elective-V	PE	40	60	3	0	0	3
	LABORATORY								
3	20MV3L1	Project work Phase –I	EEC	60	40	0	0	20	10
Total						6	0	20	16

Semester	Programme	Course Code	Course Name	L	T	P	C
III	M.E. VLSI DESIGN	20MV3E1	DATA CONVERTERS	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Explain and articulate the basic concept of sample and hold circuits.	K2	1
CO2	Design switched capacitor circuits and comparators.	K6	2
CO3	Analyze various Digital to Analog Circuits with its performance.	K4	3
CO4	Analyze various Analog to Digital Circuits with its performance.	K4	4
CO5	Generalize the different types of precision techniques used in electronic circuits	K4	5
CO6	Evaluate a situation based on application & recommended a suitable converter circuits.	K5	1,2,3,4

PRE-REQUISITE	NIL

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2				2									
CO2	3	2		2									1	
CO3	2	2	2										1	1
CO4	2	2	2										1	1
CO5	3	3		2	2		2					2		
CO6	3		2		2	2		2				2	1	1

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**SAMPLE AND HOLD CIRCUITS**	**9**
Sampling switches, Conventional open loop and closed loop sample and hold architecture, Open loop architecture with miller compensation, multiplexed input architectures, recycling architecture switched capacitor architecture.		
Topic - 2	**SWITCHED CAPACITOR CIRCUITS AND COMPARATORS**	**9**
Switched capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators.		
Topic - 3	**DIGITAL TO ANALOG CONVERTERS**	**9**
Performance metrics, reference multiplication and division, switching and logic functions in DAC, Resistor ladder DAC architecture, current steering DAC architecture.		
Topic - 4	**ANALOG TO DIGITAL CONVERTERS**	**9**
Performance metric, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.		
Topic - 5	**PRECISION TECHNIQUES**	**9**
Comparator offset cancellation, Op Amp offset cancellation, Calibration techniques, range overlap and digital correction.		

THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	Behzad Razavi, "Principles of data conversion system design", IEEE Press, 1995.
2	Walter Allan Kester, "The Data Conversion Hand Book", Analog Devices Inc., 2005.
3	Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2008.
4	Franco Malobert, "Data Converters" Springer Publications, 2007.
5	Arthur van Roermund, Herman Casier, Michiel Steyae, "Analog Circuit Design: Smart Data Converters, Filters on Chip, Multimode Transmitters", Springer Publications, 2010.
6	Mikael Gustavsson, J. Jacob Wikner, Nianxiong Tan, "CMOS Data Converters forCommunications", Kluwer Academic Publishers, 2002.

OTHER REFERENCES	
1	**https://www.youtube.com/watch?v=e9OEp5lJA4U**
2	**https://www.youtube.com/watch?v=fSz3z85aWfE**
3	**https://www.youtube.com/watch?v=icxvLWEOzEA&t=29s**
4	**https://www.youtube.com/watch?v=kkZhaDw3DUM**
5	**https://www.youtube.com/watch?v=SAcVlreweOc**

Semester	Programme	Course Code	Course Name	L	T	P	C
III	M.E. VLSI DESIGN	20MV3E2	VLSI TECHNOLOGY	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Describe the suitable crystal structure for VLSI devices, crystal growth conditions and suitable method used for particular impurity doping.	K2	1
CO2	Explain the Building layers of IC using various processing like diffusion, metallization, oxidation, epitaxial, etching lithography and fabrication of devices and circuits	K2	2
CO3	Explain process simulation.	K2	3
CO4	Explain VLSI process integration.	K2	4
CO5	Analyze Metallization and Oxidation.	K4	5
CO6	Explain packaging of VLSI devices.	K2	1,2,3,4,5

PRE-REQUISITE	VLSI DESIGN

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2	2				2		2				2	
CO2	3	2	2			2				2				2
CO3	3	2			2			2	2		2			
CO4	3	2					2		2					2
CO5	3	2	3	2		2						2	2	
CO6	3	1								2				

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**MATERIAL PROPERTIES & CRYSTAL GROWTH**	**9**
Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapour phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.		
Topic - 2	**LITHOGRAPHY AND RELATIVE PLASMA ETCHING**	**9**
Analysis of asynchronous sequential circuit - Cycles - Races - Static, Dynamic and Essential hazards - Primitive Flow Table - State Reductions and State Assignment - Design of asynchronous sequential circuits.		
Topic - 3	**DEPOSITION, DIFFUSION AND METALISATION**	**9**
Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Flick's one dimensional Diffusion Equation - Atomic Diffusion Mechanism - Measurement techniques - Range theory- Implant equipment. Annealing Shallow junction - High energy implantation - Physical vapour deposition Patterning.		
Topic - 4	**PROCESS SIMULATION AND VLSI PROCESS INTEGRATION**	**9**
Ion implantation - Diffusion and oxidation - Epitaxy - Lithography - Etching and Deposition- NMOS IC Technology - CMOS IC Technology - MOS Memory IC technology - Bipolar IC Technology - IC Fabrication.		
Topic - 5	**ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES**	**9**
Analytical Beams - Beams Specimen interactions - Chemical methods - Package types - banking design consideration - VLSI assembly technology - Package fabrication technology.		

THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	M.Sze, "VLSI Technology", Mc.Graw.Hill Second Edition. 2002.
2	Douglas A. Pucknell and Kamran Eshraghian, " Basic VLSI Design", Prentice Hall India, 2003.
3	Amar Mukherjee, "Introduction to NMOS and CMOS VLSI System design Prentice HallIndia,2000.
4	Wayne Wolf ,"Modern VLSI Design", Prentice Hall India,1998.

OTHER REFERENCES	
1	**https://www.youtube.com/watch?v=WmK1bi-nKFE&list=PLXnsjPD8-xuusZCiPKxAirmifNKoOu45X**
2	**https://www.youtube.com/watch?v=_EuN1CP8QeQ**
3	**https://www.youtube.com/watch?v=VIJGa2MVn-k**

Semester	Programme	Course Code	Course Name	L	T	P	C
III	M.E. VLSI DESIGN	20MV3E3	VLSI FOR WIRELESS COMMUNICATION	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Explain different Modulation techniques, Spread Spectrum and Receiver Architecture.	K3	1
CO2	Describe the VLSI Architecture for Wireless Systems.	K5	2
CO3	Design the various filters.	K5	3
CO4	Explain Matching Networks.	K4	4
CO5	Explain the various types of modulators and synthesizer.	K4	5
CO6	Analyze the concepts of Low Noise Amplifier, Analog to Digital Converters & Synthesizer and VLSI architecture for Wireless Systems.	K4	1,2,3,4,5

PRE-REQUISITE	NIL

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2			2				2	2			2	
CO2	3	2					2				2	2		2
CO3	3	2	2	2				2	2					
CO4	3	3				2		2	2	2				
CO5	3	2			2								2	
CO6	3	2	2	2			2					2		

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**INTRODUCTION**	**9**
Review of Modulation Schemes - BFSK- BPSK -QPSK - OQPSK - Classical Channel - Additive White Gaussian Noise - Finite Channel Bandwidth - Wireless Channel - Path Environment - Path Loss – Friis Equation - Multipath Fading - Channel Model - Envelope Fading - Frequency Selective Fading – Fast Fading - Comparison of different types of Fading- Review of Spread Spectrum - DSSS – FHSS- Principle of DSSS - Modulation - Demodulation - Performance in the presence of noise - narrowband and wideband interferences.		
Topic - 2	**RECEIVER ARCHITECTURE**	**9**
Receiver Front End - Motivations - General Design Philosophy- Heterodyne and Other architectures - Filter Design - Band Selection Filter - Image Rejection Filter - Channel Filter - Non idealities and Design Parameters - Harmonic Distortion - Intermodulation - Cascaded Nonlinear Stages - Gain Compression - Blocking - Noise - Noise Sources - Noise Figure - Design of Front end parameter for DECT.		
Topic - 3	**LOW NOISE AMPLIFIER**	**9**
Low Noise Amplifier - Matching Networks - Matching for Noise and Stability - Matching for Power - Implementation - Comparison of Narrowband and Wideband LNA - Wideband LNA Design – Narrowband LNA - Impedance matching -Power matching- Salient features of LNA -Core Amplifier Designs.		
Topic - 4	**ANALOG TO DIGITAL CONVERTERS & SYNTHESIZER**	**9**
Demodulators - Delta Modulators - Low Pass Sigma Delta Modulators - High Order Modulators - One Bit DAC and ADC -Passive Low Pass Sigma Delta Modulator - Band pass Sigma Delta Modulators - Comparison - PLL based Frequency Synthesizer.		
Topic - 5	**VLSI ARCHITECTURE FOR WIRELESS SYSTEMS**	**9**
Implementations: VLSI architecture for Multi-tier Wireless System - Hardware Design Issues for a Next generation CDMA System - Efficient VLSI Architecture for Base Band Signal processing.		

THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	Bosco Leung, "VLSI for wireless Communication", Springer, 2nd Edition, 2011.
2	Andreas F.Molisch, "Wideband wireless Digital Communication", Prentice PTR,2001.
3	George.V.Tsoulous, "Adaptive Antennas for wireless Communication", IEEE Press, Willey Publications, 2001.
4	Xiaodong Wang and H.Vincent Poor, "Wireless Communication System, Advanced Techniques for Signal Reception", Pearson Education. 2004.
5	Wolfgang Eberle, "Wireless Transceiver Systems Design", Springer, 2008.

OTHER REFERENCES	
1	**https://www.youtube.com/watch?v=Y6u2KQoPUiU**
2	**https://www.youtube.com/watch?v=cRSj4FzdXfo&list=PLC79262E787A9CBA9**
3	**https://www.youtube.com/watch?v=cIlwGFcDLhI**
4	**https://www.youtube.com/watch?v=_EuN1CP8QeQ**
5	**https://www.youtube.com/watch?v=DdoCjyTzhQY&list=PLgwJf8NK-2e6au9bX9P_bA3ywxqigCsaC**

Semester	Programme	Course Code	Course Name	L	T	P	C
III	M.E. VLSI DESIGN	20MV3E4	ANALOG VLSI CIRCUITS	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Explain and articulate the basic concepts related to CMOS technology and device modeling in analog VLSI circuits.	K2	1
CO2	Apply CMOS sub circuit and biasing circuit in analog VLSI circuits.	K3	2
CO3	Compare various stage amplifier to rate their performance in VLSI.	K4	3
CO4	Evaluate the situation based on timing issues and recommend a suitable VLSI circuits	K5	4
CO5	Analyze arithmetic building blocks to infer their limitation	K4	5
CO6	Design a VLSI equipment for a given application	K6	2,3,4,5

PRE-REQUISITE	20MV1T3 – CMOS VLSI DESIGN, 20MV2T1- LOW POWER CMOS CIRCUITS & MEMORIES, 20MV2T3 – TESTING OF VLSI CIRCUITS.

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	2		2									2	
CO2	3	2	3		2									
CO3	2	2						2					2	
CO4	2		3			2							2	
CO5		2	3								2			1
CO6	2			3					2				2	

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Mini projects
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**CMOS TECHNOLOGY AND DEVICE MODELLING**	**9**
Basic MOS semiconductor fabrication processes - other considerations of CMOS technology - MOS I/V characteristics MOS large signal model and parameters - Small signal model for the MOS transistor - Computer simulation models -Sub threshold MOS model.		
Topic - 2	**ANALOG CMOS SUB CIRCUITS AND BIASING CIRCUITS**	**9**
MOS switch - MOS diode and active resistor - Basic Current mirrors - Cascode current mirrors-active current mirrors- voltage references-supply independent biasing, temperature independent references, PTAT current generation.		
Topic - 3	**SINGLE STAGE AMPLIFIERS AND DIFFERENTIAL AMPLIFIERS**	**9**
Common source stage - Common source stage with resistive load - diode connected load - current source load - triode load - source degeneration - Source follower stage - Common -gate stage - Cascade stages - Single ended and differential operation - Basic differential pair - Common mode response - Differential pair with MOS loads. Gilbert Cell.		
Topic - 4	**TIMING ISSUES IN VLSI CIRCUITS**	**9**
General considerations-Miller effect -Association of poles with Nodes - Frequency response of Common source, Source follower, Common gate amplifiers, Cascode amplifiers and differential amplifiers - Statistical characteristics of noise - Types of Noise - Noise in single stage amplifiers -Noise in differential pairs		
Topic - 5	**DESIGN OF ARITHMETIC BUILDING BLOCKS**	**9**
Properties of feedback circuits - Feedback Topologies - Effect of loading in feedback networks - Effect of feedback on noise - Performance parameters of operational amplifiers - One stage op amp - Two stage op amp - Gain Boosting - Input range limitations - Slew rate - Power Supply Rejection- Noise in op amps - Stability and Frequency compensation.		

THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	Phillip E.Allen and Douglas R.Holberg, "CMOS Analog Circuit Design", Oxford UniversityPress, 2002
2	Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2001
3	Malcom R.Haskard and Lan C.May, "Analog VLSI Design - NMOS and CMOS", PrenticeHall, 1998.
4	Randall L Geiger, Phillip E. Allen and Noel K.Strader, "VLSI Design Techniques for Analogand Digital Circuits", Mc Graw Hill International Company, 1990.
5	K.Radhakrishna Rao," Electronics for Analog Signal Processing-I", NPTEL, Courseware, 2005

OTHER REFERENCES	
1	**https://youtu.be/DdoCjyTzhQY**
2	**http://www.brown.edu/Departments/Engineering/Labs/ddzo/async.html**
3	**https://youtu.be/oL8SKNxEaHs**
4	**https://youtu.be/QTw3V2yc6E4**
5	**https://youtu.be/DsicVlSJ0BY**

Semester	Programme	Course Code	Course Name	L	T	P	C
III	M.E. VLSI DESIGN	20MV3E5	RADIO FREQUENCY IC DEIGSN	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Explain and articulate the concepts related to RF Design and Wireless Technology	K2	1
CO2	Compare the various RF Modulation and design transmitter and receiver	K4	2
CO3	Apply the RF testing for heterodyne systems and its performance	K3	3
CO4	Analyze the BJT and MOSFET behavior at Radio frequencies.	K4	4
CO5	Evaluate a situation based application and recommend a suitable RF filters	K5	5
CO6	Design a RF mixer for a given application	K6	5

PRE-REQUISITE	VLSI TECHNOLOGY

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	1	1	2	1							2	3	
CO2	3	2	1						1		2		2	
CO3	2	1	2	2	1		2		2			1	2	
CO4	2	2	1	1		2							1	
CO5	3	1	2	2				2	1			1	3	
CO6	2	1	1	2	1				2		2	2		2

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**INTRODUCTION TO RF DESIGN AND WIRELESS TECHNOLOGY**	**9**
Design and Applications - Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance - Inter symbol interference - random processes and noise. Sensitivity and dynamic range - conversion of gains and distortion.		
Topic - 2	**RF MODULATION**	**9**
Analog and digital modulation of RF circuits - Comparison of various techniques for power efficiency - Coherent and non-coherent detection - Mobile RF communication and basics of Multiple Access techniques. Receiver and Transmitter architectures - Direct conversion and two-step transmitters		
Topic - 3	**RF TESTING**	**9**
RF testing for heterodyne - Homodyne - Image rejects - Direct IF and sub sampled receivers.		
Topic - 4	**BJT AND MOSFET BEHAVIOR AT RF FREQUENCIES**	**9**
BJT and MOSFET behaviour at RF frequencies - modelling of the transistors and SPICE model - Noise performance and limitations of devices - integrated parasitic elements at high frequencies and their monolithic implementation.		
Topic - 5	**RF CIRCUITS DESIGN**	**9**
Overview of RF Filter design - Active RF components & modelling - Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation - Low noise Amplifier design in various technologies - Design of Mixers at GHz frequency range - Various mixers- working and implementation. Oscillators- Basic topologies VCO and definition of phase noise - Noise power and trade off. Radio frequency Synthesizers- PLLS - Various RF synthesizer architectures and frequency dividers - Design issues in integrated RF filters.		

THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	John W M Rogers, Calvin Plett, "Radio Frequency Integrated Circuit Design", Second Edition,Artech House, 2010.
2	Ashok K. Sharma, "Semiconductor Memories Technology, Testing and Reliability", PrenticeHall of India Pvt. Ltd, New Delhi,1997.
3	Bahzad Razavi, "RF Microelectronics", Second Edition, Prentice Hall, 2012.

OTHER REFERENCES	
1	**https://nptel.ac.in › courses**
2	**https://www.youtube.com/watch?v=qU36Fy_aeb0**
3	**https://www.youtube.com/watch?v=TnRn3Kn_aXg**
4	**https://www.youtube.com/watch?v=oqkigUOjpGg**

Semester	Programme	Course Code	Course Name	L	T	P	C
III	M.E. VLSI DESIGN	20MV3E6	BASEBAND ALGORITHMS ON FPGA	3	0	0	3

COURSE LEARNING OUTCOMES (COs)			
After Successful completion of the course, the students should be able to		RBT Level	Topics Covered
CO1	Explain and articulate the concepts related to FPGA Technology	K2	1
CO2	Apply the various building blocks of FPGA	K3	2
CO3	Compare the various FIR and IIR filters	K4	3
CO4	Analyze the DFT and FFT algorithms	K4	4
CO5	Evaluate a situation based application and recommend a suitable communication codes in FPGA	K5	5
CO6	Design a Adaptive filters for a given application	K6	5

PRE-REQUISITE	VLSI TECHNOLOGY

CO / PO MAPPING (1 – Weak, 2 – Medium, 3 – Strong)														
COs	Programme Learning Outcomes (POs)												PSOs	
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	1	1			2						1	3	
CO2	2	1	2				2		2			2	2	
CO3	2	2	1	2	1				1		2	2	2	
CO4	3	1	1			2		2				1	1	
CO5	2	1	2	2	1				2			1	3	
CO6	3	2	1	1	2						2	1		2

COURSE ASSESSMENT METHODS		
DIRECT	1	Continuous Assessment Tests
	2	Assignment
	3	End Semester Examinations
INDIRECT	1	Course End Survey

COURSE CONTENT		
Topic - 1	**FPGA TECHNOLOGY**	**9**
Introduction to FPGA - FPGA Design flow - Programming languages - programming technology.		
Topic - 2	**BASIC BUILDING BLOCKS**	**9**
Number Representation - Binary adders - Binary dividers - Floating point arithmetic - MAC & SOP unit.		
Topic - 3	**DIGITAL FILTER IMPLEMENTATION**	**9**
FIR FILTER: Theory and structure - Filter Design - Constant coefficient - FIR Design. **IIR FILTER:** IIR theory - Coefficient computation - Implementation detail - Fast IIR filter.		
Topic - 4	**FOURIER TRANSFORM**	**9**
DFT algorithms - Goertzel algorithm - Hartley transform - Winograd DFT - Blustein chirp–z transform - Rader algorithm - FFT algorithms - Cooley-tukey - Good thomas - Winograd FFT**.**		
Topic - 5	**COMMUNICATION BLOCKS**	**9**
Error control codes - Linear block code - Convolution codes - Modulation and Demodulation - Adaptive filters - LMS - RLS - Decimator and Interpolator - High Decimation Rate filters.		

THEORY	**45**		**TUTORIAL**	**0**		**PRACTICAL**	**0**		**TOTAL**	**45**

BOOK REFERENCES	
1	Uwe.Meyer-Baese, “Digital Signal Processing with Field Programmable Gate Arrays”,Springer, Third edition, May 2007.
2	Keshab K. Parhi, “VLSI Digital Signal Processing systems, Design and implementation”, Wiley,Inter Science, 1999.
3	John G. Proakis, “Digital Communications,” Fourth Ed. McGraw Hill International Edition,2000.
4	Michael John Sebastian Smith, “ Applications Specific Integrated Circuits”, PearsonEducation, Ninth Indian reprint,13th edition,2004.
5	Sophocles J. Orfanidis, “Introduction to Signal Processing”, Prentice Hall, 1996

OTHER REFERENCES	
1	**https://nptel.ac.in › courses**
2	**https://www.youtube.com/watch?v=CLUoWkJUnN0**
3	**https://www.youtube.com/watch?v=jbOjWp4C3V4**
4	**https://www.youtube.com/watch?v=jVYs-GTqm5U g**
5	**https://www.youtube.com/watch?v=VySEvtpM_To**